Datasheet

APM32F402xB

Arm® Cortex® -M4F core-based 32-bit MCU

Version: V1.1

1 Product characteristics

Core

- 32-bit Arm® Cortex®-M4F core
- Up to 120MHz operating frequency

Memory and interface

- Flash: Up to 128KB
- SRAM: Up to 32KB

Clock

- HSECLK: 4~16MHz external crystal/ceramic oscillator supported
- LSECLK: 32.768kHz crystal/ceramic oscillator supported
- HSICLK: 8MHz RC oscillator calibrated by factory
- LSICLK: 40kHz RC oscillator supported
- PLL: Phase locked loop, 2~16 times of frequency supported

Power supply and power supply management

- V_{DD} range: 2.0～3.6V
- V_{DDA} range: 2.0～3.6V
- V_{BAT} range of backup domain power supply: 1.8V～3.6V
- Power-on/power-down reset (POR/PDR) supported
- Programmable voltage detector (PVD) supported

Low-power mode

- Sleep, stop and standby modes supported

DMA

- Two DMA, 7 channels for DMA1 and 5 channels for DMA2

Debugging interface

- JTAG
- SWD

I/O

- Up to 51 I/O
- All I/O can be mapped to external interrupt vector

Communication peripherals

- 1 I2C interface (1Mbit/s), supporting SMBus/PMBus
- 3 USART, 1 UART, supporting ISO7816, LIN and IrDA functions
- 2 SPI (1 reusable I2S), with a maximum transmission speed of 18Mbps
- 2 CAN, with a maximum baud rate of communication of 1Mbit/s
- 1 USB OTG-FS

Analog peripherals

- 2 12-bit ADC

Timer

- 2 16-bit advanced timers TMR1/8 that can provide 7-channel PWM output, support dead zone generation and braking input functions
- 1 32-bit general-purpose timer TMR2, 3 16-bit general-purpose timers TMR3/4/5, each with up to 4 independent channels to support input capture, output compare, PWM, pulse count and other functions
- 2 watchdog timers: One independent watchdog IWDT and one window watchdog WWDT
- 1 24-bit autodecrement system timer Sys Tick Timer

RTC

- Support calendar function

84Bytes backup register

CRC computing unit

96-bit unique device ID

Chip package

- QFN36/QFN48/LQFP48/LQFP64

Contents

2 Product information

See the following table for APM32F402xB product functions and peripheral configuration.

Table 1 Functions and Peripherals of APM32F402xB Series Chips

Product		**APM32F402xB**			
Model		TBUx	CBTx	CBUx	RBTx
Package		QFN36	LQFP48	QFN48	LQFP64
Core and maximum working frequency		Arm® 32-bit Cortex®-M4F@120MHz			
Working voltage		2.0~3.6V			
Flash (KB)		128	128	128	128
SRAM(KB)		32	32	32	32
GPIOs		26	37	37	51
Communication interface	USART/UART	2/0	3/0	3/0	3/1
	SPI/I2S	1/1	2/1		
	I2C	1			
	USB OTG-FS	1			
	CAN	2			
Timer	16-bit advanced	2			
	32-bit general	1			
	16-bit general	3			
	System tick timer	1			
	Watchdog	2			
Real-time Clock		1			
12-bit ADC	Unit	2			
	Channel	10			16
Operating temperature		Ambient temperature: -40°C to 85°C/-40°C to 105°C Junction temperature: -40°C to 105°C/-40°C to 125°C			

Note：When x is 6, the ambient temperature is -40℃ to 85℃, and the junction temperature is -40℃ to 105℃.
When x is 7, the ambient temperature is -40℃ to 105℃, and the junction temperature is -40℃ to 125℃.

3 Pin information

3.1 Pin distribution

Figure 1 Distribution Diagram of APM32F402xB Series LQFP64 Pins

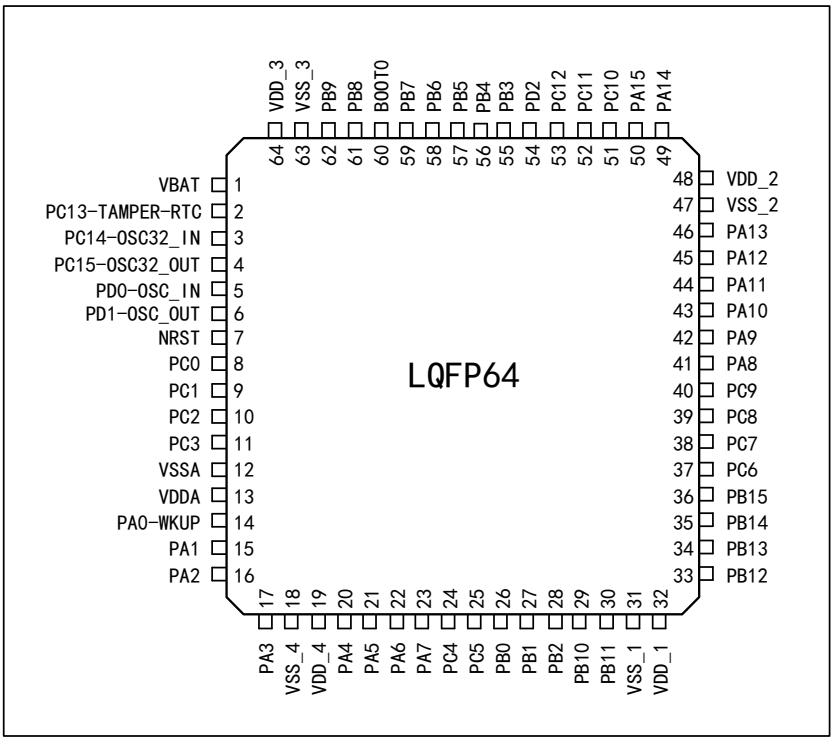


Figure 2 Distribution Diagram of APM32F402xB Series LQFP48 Pins

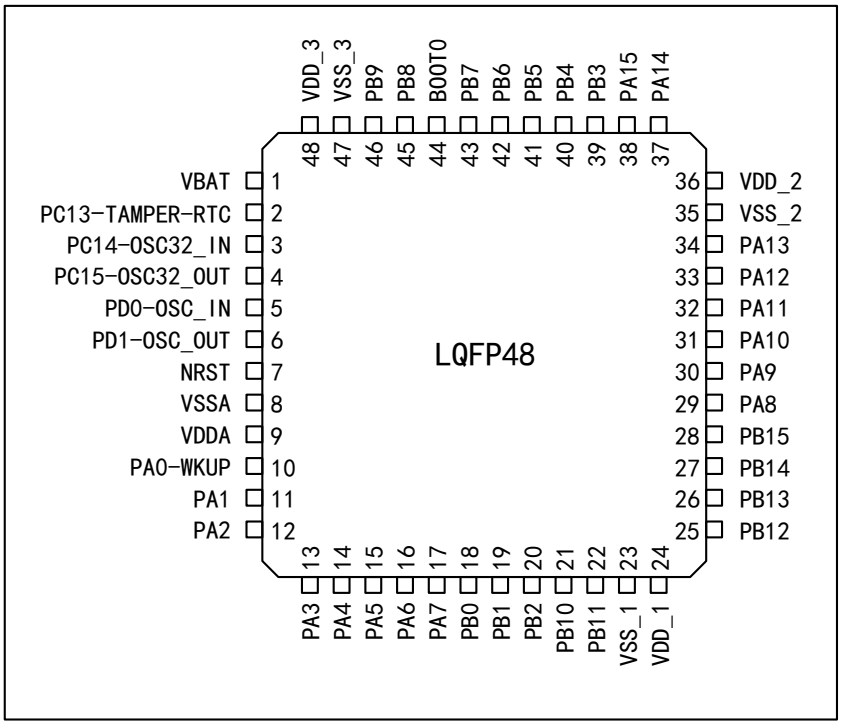


Figure 3 Distribution Diagram of APM32F402xB Series QFN48 Pins

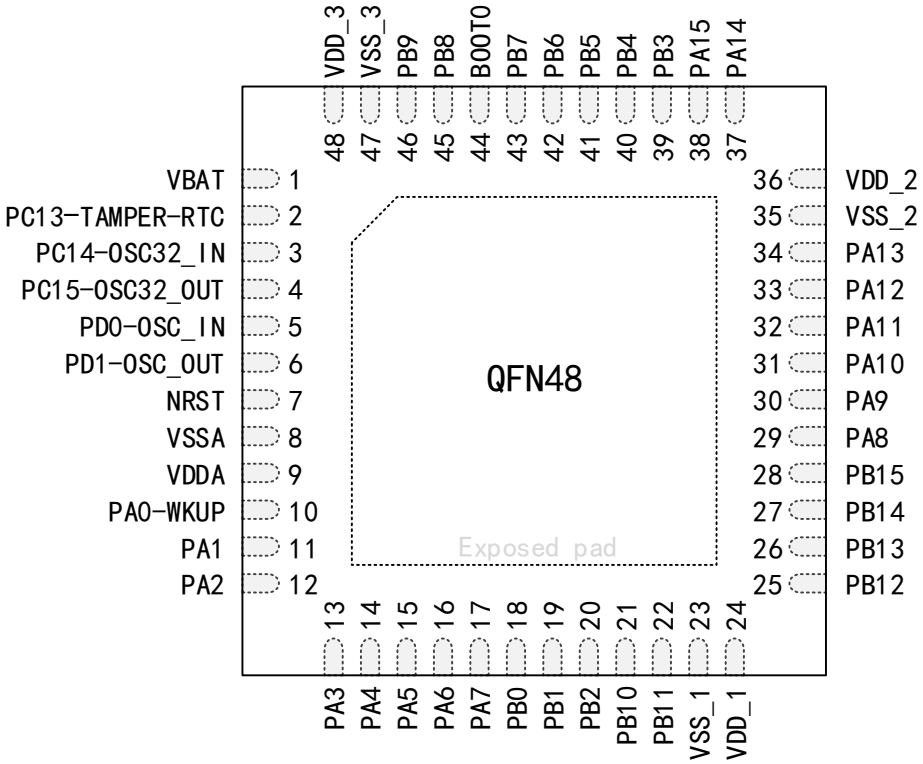
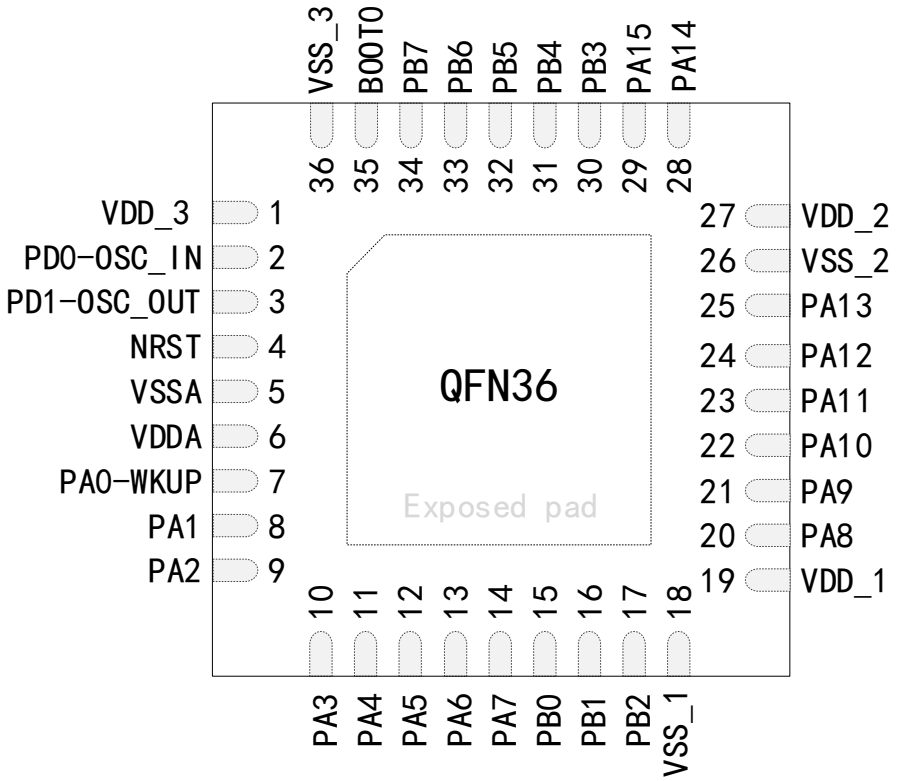


Figure4 Distribution Diagram of APM32F402xB Series QFN36 Pins



3.2 Pin functional description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name		Abbreviations	Definitions
Pin name		Unless otherwise specified in the bracket below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type		P	Power supply pin
		I	Only input pin
		I/O	I/O pin
I/O structure		5T	FT I/O
		5Tf	FT I/O, FM+ function
		STDA	3.3V standard I/O, directly connected to ADC
		STD	3.3V standard I/O
		B	Dedicated Boot0 pin
		RST	Bidirectional reset pin with built-in weak pull-up resistor
Caution		Unless otherwise specified in the notes, all I/O is set as floating input during and after reset	
Pin function	Default multiplexing function	Select/enable this function directly through peripheral register	
	Redefining function	Select this function through AFIO remapping register	

Table 3 APM32F402xB Pin Function Description

Name (function after reset)	Type	Structure	Default multiplexing function	Redefining function	QFN36	QFN48/LQFP48	LQFP64
V_{BAT}	P	-	-	-	-	1	1
PC13-TAMPER-RTC (PC13)	I/O	STD	TAMPER_RTC	-	-	2	2
PC14-OSC32_IN (PC14)	I/O	STD	OSC32_IN	-	-	3	3
PC15-OSC32_OUT (PC15)	I/O	STD	OSC32_OUT	-	-	4	4
OSC_IN	I	STD	-	PD0	2	5	5
OSC_OUT	O	STD	-	PD1	3	6	6
NRST	I/O	RST	-	-	4	7	7

Name (function after reset)	Type	Structure	Default multiplexing function	Redefining function	QFN36	QFN48/LQFP48	LQFP64
PC0	I/O	STDA	ADC12_IN10	-	-	-	8
PC1	I/O	STDA	ADC12_IN11	-	-	-	9
PC2	I/O	STDA	ADC12_IN12	-	-	-	10
PC3	I/O	STDA	ADC12_IN13	-	-	-	11
V_{SSA}	P	-	-	-	5	8	12
V_{DDA}	P	-	-	-	6	9	13
PA0-WKUP (PA0)	I/O	STDA	WKUP, USART2_CTS, ADC12_IN0, TMR2_CH1_ETR, TMR5_CH1, TMR8_ETR	-	7	10	14
PA1	I/O	STDA	USART2_RTS, ADC12_IN1, TMR5_CH2, TMR2_CH2	-	8	11	15
PA2	I/O	STDA	USART2_TX, TMR5_CH3, ADC12_IN2, TMR2_CH3	-	9	12	16
PA3	I/O	STDA	USART2_RX, TMR5_CH4, ADC12_IN3, TMR2_CH4	-	10	13	17
V_{SS_4}	P	-	-	-	-	-	18
V_{DD_4}	P	-	-	-	-	-	19
PA4	I/O	STDA	SPI1_NSS, USART2_CK, ADC12_IN4	-	11	14	20
PA5	I/O	STDA	SPI1_SCK, ADC12_IN5	-	12	15	21
PA6	I/O	STDA	SPI1_MISO, TMR8_BKIN, ADC12_IN6 TMR3_CH1	TMR1_BKIN	13	16	22
PA7	I/O	STDA	SPI1_MOSI, TMR8_CH1N,	TMR1_CH1N	14	17	23

Name (function after reset)	Type	Structure	Default multiplexing function	Redefining function	QFN36	QFN48/LQFP48	LQFP64
			ADC12_IN7, TMR3_CH2				
PC4	I/O	STDA	ADC12_IN14	-	-	-	24
PC5	I/O	STDA	ADC12_IN15	-	-	-	25
PB0	I/O	STDA	ADC12_IN8, TMR3_CH3, TMR8_CH2N	TMR1_CH2N	15	18	26
PB1	I/O	STDA	ADC12_IN9, TMR3_CH4, TMR8_CH3N	TMR1_CH3N	16	19	27
PB2 (PB2,BOOT1)	I/O	5T	-	-	17	20	28
PB10	I/O	5T	USART3_TX	TMR2_CH3	-	21	29
PB11	I/O	5T	USART3_RX	TMR2_CH4	-	22	30
V_{SS_1}	P	-	-	-	18	23	31
V_{DD_1}	P	-	-	-	19	24	32
PB12	I/O	5T	SPI2_NSS, I2S2_WS, USART3_CK, TMR1_BKIN, CAN2_RX	-	-	25	33
PB13	I/O	5T	SPI2_SCK, I2S2_CK, USART3_CTS, TMR1_CH1N, CAN2_TX	-	-	26	34
PB14	I/O	5T	SPI2_MISO, TMR1_CH2N, USART3_RTS	-	-	27	35
PB15	I/O	5T	SPI2_MOSI, I2S2_SD, TMR1_CH3N	-	-	28	36
PC6	I/O	5T	I2S2_MCK, TMR8_CH1	TMR3_CH1	-	-	37
PC7	I/O	5T	TMR8_CH2	TMR3_CH2	-	-	38
PC8	I/O	5T	TMR8_CH3	TMR3_CH3	-	-	39
PC9	I/O	5T	TMR8_CH4	TMR3_CH4	-	-	40
PA8	I/O	5T	USART1_CK,	-	20	29	41

Name (function after reset)	Type	Structure	Default multiplexing function	Redefining function	QFN36	QFN48/LQFP48	LQFP64
			TMR1_CH1, MCO, OTG_FS_SOF				
PA9	I/O	5T	USART1_TX, TMR1_CH2, OTG_FS_VBUS	-	21	30	42
PA10	I/O	5T	USART1_RX, TMR1_CH3, OTG_FS_ID	-	22	31	43
PA11	I/O	5T	USART1_CTS, CAN1_RX, TMR1_CH4, OTG_FS_DM	-	23	32	44
PA12	I/O	5T	USART1_RTS, CAN1_TX, TMR1_ETR, OTG_FS_DP	-	24	33	45
PA13 (JTMS,SWDIO)	I/O	5T	-	PA13	25	34	46
V_{SS_2}	P	-	-	-	26	35	47
V_{DD_2}	P	-	-	-	27	36	48
PA14 (JTCK,SWCLK)	I/O	5T	-	PA14	28	37	49
PA15 (JTDI)	I/O	5T	-	TMR2_CH1_ETR, PA15, SPI1_NSS	29	38	50
PC10	I/O	5T	UART4_TX	USART3_TX	-	-	51
PC11	I/O	5T	UART4_RX	USART3_RX	-	-	52
PC12	I/O	5T		USART3_CK	-	-	53
PD2	I/O	5T	TMR3_ETR	-	-	-	54
PB3 (JTDO)	I/O	5T		PB3, TRACESWO, TMR2_CH2, SPI1_SCK	30	39	55
PB4 (NJTRST)	I/O	5T		PB4, TMR3_CH1, SPI1_MISO	31	40	56
PB5	I/O	5T	I2C1_SMBAI	TMR3_CH2, SPI1_MOSI,	32	41	57

Name (function after reset)	Type	Structure	Default multiplexing function	Redefining function	QFN36	QFN48/LQFP48	LQFP64
				CAN2_RX			
PB6	I/O	5T	I2C1_SCL, TMR4_CH1	USART1_TX, CAN2_TX	33	42	58
PB7	I/O	5T	I2C1_SDA, TMR4_CH2	USART1_RX	34	43	59
BOOT0	I	5T	-	-	35	44	60
PB8	I/O	5T	TMR4_CH3	I2C1_SCL, CAN1_RX	-	45	61
PB9	I/O	5T	TMR4_CH4	I2C1_SDA, CAN1_TX	--	46	62
V_{SS_3}	P	-	-	-	36	47	63
V_{DD_3}	P	-	-	-	1	48	64

Note:

(1) The functions that can be used depend on the selected model. For models with a few peripheral modules, they always include functional modules of small numbers. For example, when a certain model only has 1 SPI and 2 USART, they are SPI1, USART1, and USART2.

(2) The PC13, PC14, and PC15 pins are powered by the power switch, which can only absorb limited current (3mA). Therefore, there are the following restrictions on these three pins when they serve as output pins: only one pin serves as the output at the same time, and the pin serving as an output pin can only work in 2MHz mode, with an maximum driving load of 30pF, and cannot serve as the current source (e.g. driving LED).

(3) These pins are in the main functional state when the backup area is powered on for the first time, and even if they are reset afterwards, the state of these pins is controlled by the backup area registers (these registers will not be reset by the main reset system). For specific information on how to control these IO ports, please refer to the Battery Backup Area and BAKPR Register in the *User Manual*.

(4) This multiplexing function can be configured to other pins by software (if the corresponding package model has this pin). For details, please refer to the Multiplexing Function I/O and Debugging Settings of the *User Manual*.

(5) The pins 5 and 6 of the LQFP64 package are configured as OSC_IN and OSC_OUT function pins by default after the chip is reset. The software can reset these two pins as PD0 and PD1 functions. For more detailed information, please refer to the Multiplexing Function I/O and Debugging Settings of the *Manual*.

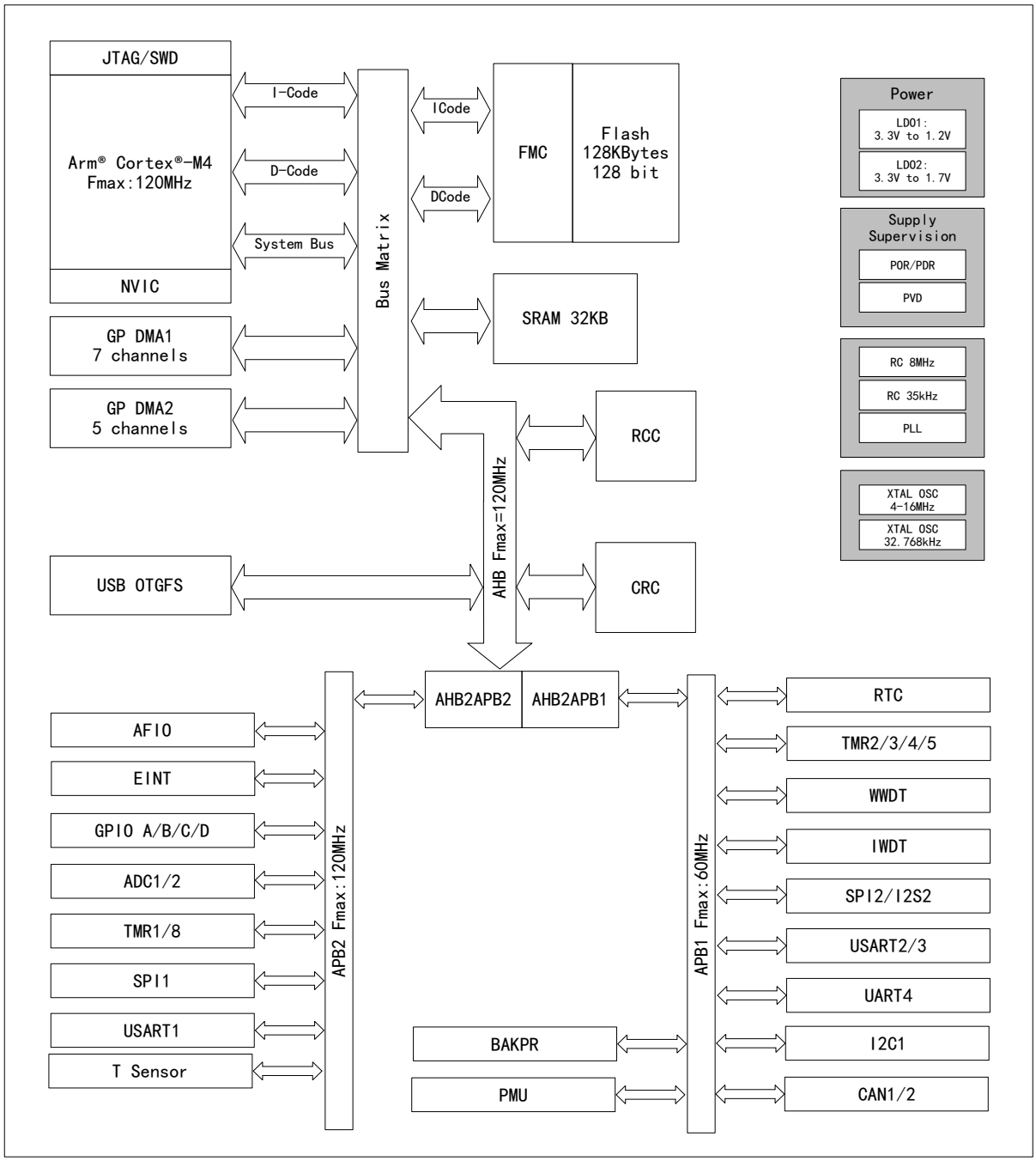
4 Functional description

This chapter mainly introduces the system architecture, interrupt, on-chip memory, clock, power supply and peripheral features of APM32F402xB series products; for information about the Arm® Cortex®-M4F core, please refer to the *Arm® Cortex®-M4F Technical Reference Manual*, which can be downloaded from ARM's website.

4.1 System Architecture

4.1.1 System Block Diagram

Figure 5 APM32F402xB System Block Diagram



4.1.2 Address Mapping

Table 4 Address Mapping Table of APM32F402xB Series

Area	Start address	Peripheral name
Code	0x0000 0000	Code mapping area
Code	0x0002 0000	Reserved

Area	Start address	Peripheral name
Code	0x0800 0000	Flash
Code	0x0802 0000	Reserved
Code	0x1FFF 6000	ROM area
Code	0x1FFF B000	Reserved
Code	0x1FFF E400	System memory area
Code	0x1FFF F800	Option byte
Code	0x1FFF F810	Reserved
SRAM	0x2000 0000	SRAM
SRAM	0x2000 8000	Reserved
APB1 bus	0x4000 0000	TMR2
APB1 bus	0x4000 0400	TMR3
APB1 bus	0x4000 0800	TMR4
APB1 bus	0x4000 0C00	TMR5
APB1 bus	0x4000 1000	Reserved
APB1 bus	0x4000 2800	RTC
APB1 bus	0x4000 2C00	WWDT
APB1 bus	0x4000 3000	IWDT
APB1 bus	0x4000 3400	Reserved
APB1 bus	0x4000 3800	SPI2/I2S2
APB1 bus	0x4000 3C00	Reserved
APB1 bus	0x4000 4400	USART2
APB1 bus	0x4000 4800	USART3
APB1 bus	0x4000 4C00	UART4
APB1 bus	0x4000 5000	Reserved
APB1 bus	0x4000 5400	I2C1
APB1 bus	0x4000 5800	Reserved
APB1 bus	0x4000 6400	CAN1
APB1 bus	0x4000 6800	CAN2
APB1 bus	0x4000 6C00	BAKPR
APB1 bus	0x4000 7000	PMU
—	0x4000 7400	Reserved
APB2 bus	0x4001 0000	AFIO
APB2 bus	0x4001 0400	EINT
APB2 bus	0x4001 0800	Port A
APB2 bus	0x4001 0C00	Port B
APB2 bus	0x4001 1000	Port C
APB2 bus	0x4001 1400	Port D
APB2 bus	0x4001 1800	Reserved

Area	Start address	Peripheral name
APB2 bus	0x4001 2400	ADC1
APB2 bus	0x4001 2800	ADC2
APB2 bus	0x4001 2C00	TMR1
APB2 bus	0x4001 3000	SPI1
APB2 bus	0x4001 3400	TMR8
APB2 bus	0x4001 3800	USART1
—	0x4001 3C00	Reserved
AHB bus	0x4002 0000	DMA1
AHB bus	0x4002 0400	DMA2
AHB bus	0x4002 0800	Reserved
AHB bus	0x4002 1000	RCM
AHB bus	0x4002 1400	Reserved
AHB bus	0x4002 2000	Flash interface
AHB bus	0x4002 2400	Reserved
AHB bus	0x4002 3000	CRC
AHB bus	0x4002 3400	Reserved
AHB bus	0x5000 0000	USB_OTG_FS
—	0x5004 0000	Reserved
Core	0xE000 0000	M4F core peripheral

4.1.3 Startup configuration

At startup, the user can select one of the following three boot modes by setting the high and low levels of the Boot pin:

- Boot from main memory
- Boot from BootLoader
- Boot from built-in SRAM

To boot from BootLoader, the user can choose to reprogram the user Flash through any of the following serial interfaces:

- USART1(PA9/PA10)
- USART2(PA2/PA3)
- I2C1(PB6/PB7)
- SPI1(PA4/PA5/PA6/PA7)
- CAN2(PB5/PB6)
- USB OTG_FS slave device mode (PA11/PA12)

4.2 Core

The core of APM32F402xB is Arm® Cortex®-M4F. Based on this platform, the development cost is low and the power consumption is low. It can provide excellent computing performance and advanced system interrupt response, and is compatible with all Arm tools and software.

4.3 Interrupt Controller

4.3.1 Nested Vectored Interrupt Controller (NVIC)

It embeds a nested vectored interrupt controller (NVIC) able to handle up to 66 maskable interrupt channels (not including 16 interrupt lines of Arm® Cortex®-M4F) and 16 priority levels. The interrupt vector entry address can be directly transmitted to the core, so that the interrupt response processing with low delay can give priority to the late higher-priority interrupt.

4.3.2 External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 19 edge detectors, and each detector includes the edge detection circuit and interrupt/event request generation circuit; each detector can be configured as rising edge trigger, falling edge trigger or both and can be masked independently. Up to 51 GPIO can be connected to 16 external interrupt lines.

4.4 Memory

The on-chip memory includes main memory area, SRAM and information block; the information block includes system memory area and option byte; the system memory area stores BootLoader, 96-bit unique device ID and capacity information of main memory area; the system memory area has been written to the program when leaving the factory and cannot be erased.

Table 5 On-chip Memory Area

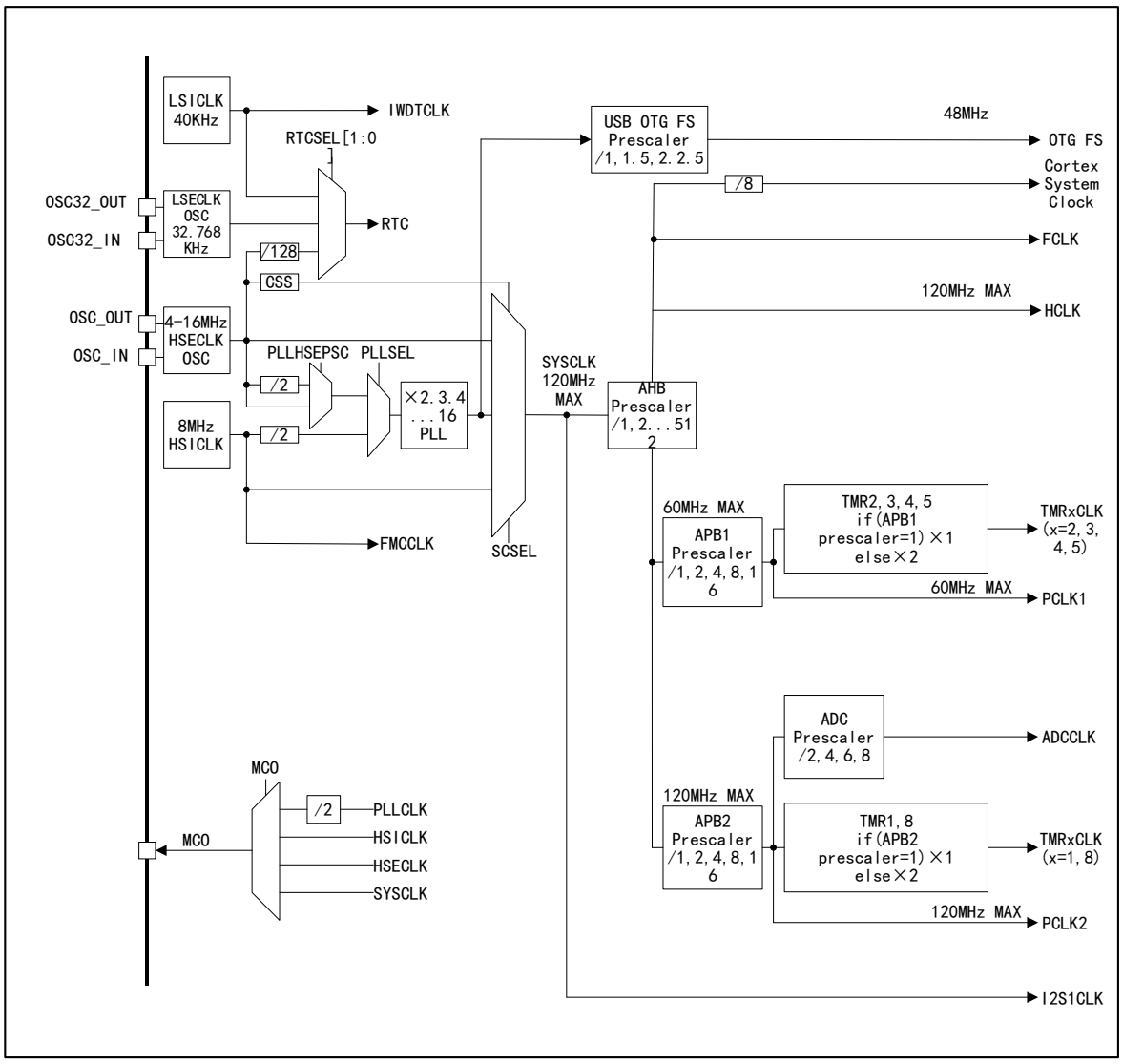
Memory	Maximum capacity	Function
Main memory area	128KB	Store user programs and data
SRAM	32KB	CPU can access at 0 wait cycle (read/write)
ROM	20KB	Store BootLoader
System memory area	5KB	Store BootLoader, 96-bit unique device ID, and main memory area capacity information
Option byte	16Bytes	Configure main memory area read-write protection and MCU working mode

4.5 Clock

4.5.1 Clock tree

Clock tree of APM32F402xB is shown in the figure below:

Figure 6 APM32F402xB Clock Tree



4.5.2 Clock source

The clock source is divided into high-speed clock and low-speed clock according to the speed; the high-speed clock includes HSICLK and HSECLK, and the low-speed clock includes LSECLK and LSICLK; the clock source is divided into internal clock and external clock according to the chip inside/outside; the internal clock includes HSICLK and LSICLK, and the external clock includes HSECLK and LSECLK, among which HSICLK is calibrated to an accuracy of ±1% by the factory.

4.5.3 System clock

HSICLK, PLLCLK and HSECLK can be selected as system clock; the clock source of PLLCLK can be HSICLK or HSECLK; the requirred system clock can be obtained by configuring PLL clock multiplier factor and frequency division factor.

When the product is reset and started, HSICLK is selected as the system clock by default, and then the user can choose one of the above clock sources as the system clock by himself. When HSECLK failure is detected, the system will automatically switch to the HSICLK, and if the

interrupt is enabled, the software can receive the related interrupt.

4.5.4 Bus clock

AHB, APB1 and APB2 buses are built in. The clock source of AHB is SYSCLK, and the clock source of APB1 and APB2 is HCLK; the required clock can be obtained by configuring the frequency division factor. The maximum frequency of AHB and high-speed APB2 is 120MHz, and that of APB1 is 60MHz.

4.6 Power supply and power supply management

4.6.1 Power supply scheme

Table 6Power Supply Scheme

Name	Voltage range	Description
V_{DD}	2.0～3.6V	Power the I/O (see the pin distribution diagram for specific IO) and internal voltage regulator through V_{DD} pin.
V_{DDA}/V_{SSA}	2.0～3.6V	Supply power to ADC, reset module, RC oscillator and PLL analog part; when ADC is used, V_{DDA} should not be less than 2.4V, and V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively.
V_{BAT}	1.8～3.6V	When V_{DD} is disabled, power the RTC, external 32kHz oscillator and backup register through the internal power switch.

4.6.2 Voltage regulator

Table 7Operating Mode of Voltage Regulator

Name	Description
Main mode (MR)	Used in run mode
Low-power mode (LPR)	Used in stop mode
Power-down mode	Used in standby mode; then the voltage regulator has high-impedance output, the core circuit is powered down, and all data of registers and SRAM will be lost.

Note: The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

4.6.3 Power supply voltage detector

Power-on reset (POR) and power-down reset (PDR) circuits are integrated inside the product. These two circuits are always in working condition. When the power-down reset circuit monitors that the power supply voltage is lower than the specified threshold value ($V_{POR/PDR}$), even for the external reset circuit, the system will remain reset.

The product has a built-in programmable voltage detector (PVD) that can monitor V_{DD} and compare it with V_{PVD} threshold. When V_{DD} is outside the V_{PVD} threshold range and the interrupt is enabled, an interrupt will be generated and the MCU can be set to a safe state through the interrupt service program.

4.7 Low-power mode

APM32F402xB supports three low-power modes, namely, sleep mode, stop mode and standby mode, and there are differences in power, wake-up time and wake-up method among these three modes. The low-power mode can be selected according to the actual application requirements.

Table 8 Low-power Mode

Mode	Description
Sleep mode	The core stops working, all peripherals are working, and it can be woken up through interrupts/events.
Stop mode	Under the condition that SRAM and register data is not lost, the lowest power can be reached in stop mode; The clock of the internal 1.3V power supply module will stop, HSECLK crystal resonator, HSICLK and PLL will be disabled, and the voltage regulator can be configured in normal mode or low-power mode; Any external interrupt line can wake up MCU, and the external interrupt lines include one of the 16 external interrupt lines, PVD output, RTC and USB_OTG_FS.
Standby mode	The power in this mode is the lowest; The internal voltage regulator is disabled, all 1.2V power supply modules are powered down, HSECLK crystal resonator, HSICLK, and PLL clocks are disabled, SRAM and register data disappears, RTC area and backup register contents remain, and the standby circuit still works; The external reset signal on NRST, IWDT reset, rising edge on WKUP pin or RTC event will wake MCU out of standby mode.

4.8 DMA

2 DMA are built in, DMA1 supports 7 channels and DMA2 supports 5 channels. Each channel supports multiple DMA requests, but only 1 DMA request is allowed to enter the DMA channel at a time. The peripherals supporting DMA requests are ADC, SPI, USART, I2C, and TMRx. Four levels of DMA channel priority can be configured. Data transmission of "Memory → Memory, Memory → Peripheral, Peripheral → Memory" is supported (memory includes Flash and SRAM).

4.9 GPIO

GPIO can be configured as general-purpose input, general-purpose output, multiplexing function and analog input and output. The general-purpose input can be configured as floating input, pull-up input and pull-down input; the general-purpose output can be configured as push-pull output and open-drain output; the multiplexing function can be used for digital peripherals; the analog input and output can be used for analog peripherals and low-power mode; the enable and disable pull-up/pull-down resistor can be configured; the speeds of 2MHz, 10MHz, and 50MHz can be configured; the higher the speed is, the greater the power consumption and the noise are.

4.10 Communication peripherals

4.10.1 USART/UART

Up to 4 universal synchronous/asynchronous receiver transmitters are built in the chip. The USART1 interface can communicate at a rate of 4.5Mbit/s, while other USART/UART interfaces can communicate at a rate of 2.25Mbit/s. All USART/UART interfaces can configure baud rate, parity check bit, stop bit, and data bit length; all USART/UART can support DMA. The function differences of USART/UART are shown in the following table:

Table 9 USART/UART Function Differences

USART mode/function	USART1	USART2	USART3	UART4
Hardware flow control of modem	√	√	√	—
Synchronous mode	√	√	√	—
Smart card mode	√	√	√	—
IrDASIR coder-encoder functions	√	√	√	√
LIN mode	√	√	√	√
Single-line half-duplex mode	√	√	√	√
Support DMA function	√	√	√	√

Note: √=support.

4.10.2 I2C

I2C1 can work in multiple-master or slave modes, supports 7-bit or 10-bit addressing, and supports dual-slave addressing in 7-bit slave mode; the communication rate supports standard mode (up to 100kbit/s) and fast mode (up to 400kbit/s); hardware CRC generator/checker are built in; they can operate with DMA and support SMBus 2.0 version/PMBus.

4.10.3 SPI/I2S

2 SPI interfaces are built in, which support full-duplex and half-duplex communication in master mode and slave mode, can use DMA controller, and can configure 4~16 bits per frame, and communicate at a rate of up to 18Mbit/s.

One I2S is built in (multiplexed with SPI2), supports half-duplex communication in master mode and slave mode, supports synchronous transmission, and can be configured with 16-bit, 24-bit and 32-bit data transfer with 16-bit or 32-bit resolution. The configurable range of audio sampling rate is 8kHz~48kHz; when one or two I2S interfaces are configured as the master mode, the master clock can be output to external DAC or decoder (CODEC) at 256 times of the sampling frequency.

4.10.4 CAN

2 CAN are built in (CAN1 and CAN2 can be used at the same time), compatible with 2.0A and 2.0B (active) specifications, which can communicate at a rate of up to 1Mbit/s. It can receive

and transmit standard frame of 11-bit identifier and extended frame of 29-bit identifier. It has 3 sending mailboxes, 2 3-level receive FIFO, and 28 adjustable filters.

4.10.5 USB_OTG_FS

One USB_OTG_FS controller is built in the product. It supports both host and slave functions and complies with the On-The-Go supplementary standard of USB 2.0 specification. It can also be configured as "Host only" or "Slave only" mode, and fully complies with USB 2.0 specification. OTG_FS clock (48MHz) is obtained through frequency division of PLL.

4.11 Analog peripherals

4.11.1 ADC

2 built-in ADC with 12-bit accuracy, up to 16 external channels and 2 internal channels for each ADC. The internal channels measure the temperature sensor voltage and reference voltage respectively. A/D conversion mode for each channel includes single, continuous, scan or intermittent modes, and ADC conversion results can be left-aligned or right-aligned and stored in 16-bit data register. It supports analog watchdog and DMA.

4.11.1.1 Temperature sensor

1 temperature sensor (TSensor) is built in, which is internally connected with ADC_IN16 channel. The voltage generated by the sensor changes linearly with temperature, and the converted voltage value can be obtained by ADC and converted into temperature.

Table 10 Calibration Value of Tsensor

Calibration value name	Description	Memory address
V_{sensor_CAL1}	At 25° C, original data collected when V_{DDA}=3.3V	0x1FFF F7FC - 0x1FFF F7FD

4.11.1.2 Internal reference voltage

Built-in reference voltage V_{REFINT}, internally connected to ADC_IN17 channel; V_{REFINT} can be obtained through ADC; V_{REFINT} provides stable voltage output for ADC.

Table 11 Internal Reference Voltage Calibration Value

Calibration value name	Description	Memory address
V_{REFINT_CAL}	At 25℃(±5℃), Original data collected when V_{DDA} =3.3V (±10mV)	0x1FFF F7FA - 0x1FFF F7FB

4.12 Timer

Built-in 2 16-bit advanced timers (TMR1/8), 4 universal timers (TMR2/3/4/5), 1 independent watchdog timer, 1 window watchdog timer, and 1 system tick timer.

Watchdog timer can be used to detect whether the program is running normally.

The system tick timer is the peripheral of the core with automatic reloading function. When the

counter is 0, it can generate a maskable system interrupt, which can be used for real-time operating system and general delay.

Table 12 Function Comparison between Advanced/General-purpose/Basic and System Tick Timers

Timer type	**System tick timer**	**General-purpose timer**				**Advanced timer**	
Timer name	Sys Tick Timer	TMR2	TMR3	TMR4	TMR5	TMR1	TMR8
Counter resolution	24 bits	32 bits	16 bits			16 bits	
Counter type	Down	Up, down, up/down				Up, down, up/down	
Prescaler factor	-	Any integer between 1 and 65536				Any integer between 1 and 65536	
Generate DMA request	-	Can				Can	
Capture/compare register	-	4				4	
Complementary output	-	None				Yes	
Pin characteristics	-	There are 5 pins in total: 1-way external trigger signal input pins, 4-way channel (non-complementary channel) pins				There are 9 pins in total: 1-way external trigger signal input pins, 1-way braking input signal pins, 3 pairs of complementary channel pins, 1-way channel (non-complementary channel) pin	
Function Description	Special for real-time operating system Automatic reloading function supported When the counter is 0, a maskable system interrupt can be generated Programmable clock source	Synchronization or event chaining function provided The counter in debug mode can be frozen. -Can be used to generate PWM output Each timer has an independent DMA request mechanism. It can handle incremental encoder signals.				It has complementary PWM output with dead band insertion When configured as a 16-bit standard timer, it has the same function as the TMRx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0~100%). In debug mode, timers can be frozen, and PWM output is disabled. Synchronization or event chaining function is provided.	

Table 13 Independent Watchdog and Window Watchdog Timers

Name	Counter resolution	Counter type	Prescaler factor	Functional description
Independent watchdog	12 bits	Down	4/8/16/32/64/128/256	The clock is provided by an internally independent RC oscillator of 40kHz, which is independent of the master clock, so it can run in stop and standby modes. The whole system can be reset in case of any problems. It can provide timeout management for applications as a free-running timer. It can be configured as a software or hardware startup watchdog through option bytes. The counter in debug mode can be frozen.
Window watchdog	7 bits	Down	-	Can be set for free running. The whole system can be reset in case of any problems. Driven by the master clock, it has early warning interrupt function; The counter in debug mode can be frozen.

4.13 RTC

1 RTC is built in, and there are LSECLK signal input pins (OS32_IN and OS32_OUT) and 1 TAMP input signal detection pin (TAMP); the clock source can select external 32.768kHz external crystal oscillator, resonator or oscillator, LSICLK and HSECLK/128; it is powered by V_{DD} by default; when V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and RTC configuration and time data will not be lost; RTC configuration and time data will not be lost in case of system reset, software reset and power-on reset; it supports alarm and calendar functions.

4.13.1 Backup register

84KB backup registers are built in, and are powered by V_{DD} by default; when V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and the data in backup register will not be lost; the data in backup registers will not be lost in case of system reset, software reset and power-on reset.

4.14 CRC

1 CRC (cyclic redundancy check) computing unit is built in, which can generate CRC codes and operate 8-bit, 16-bit and 32-bit data.

5 Electrical Characteristics

5.1 Test Conditions of Electrical Characteristics

5.1.1 Maximum and minimum values

Unless otherwise specified, all products are tested on the production line at T_A=25℃. Its maximum and minimum values can support the worst ambient temperature, power supply voltage and clock frequency.

The notes at the bottom of each table indicate that the data are obtained through comprehensive evaluation, design simulation or process characteristics and are not tested on the production line; on the basis of comprehensive evaluation, after passing the sample test, the average value is taken and three times the standard deviation (average $\pm 3\Sigma$) is added or subtracted to get the maximum and minimum values.

5.1.2 Typical value

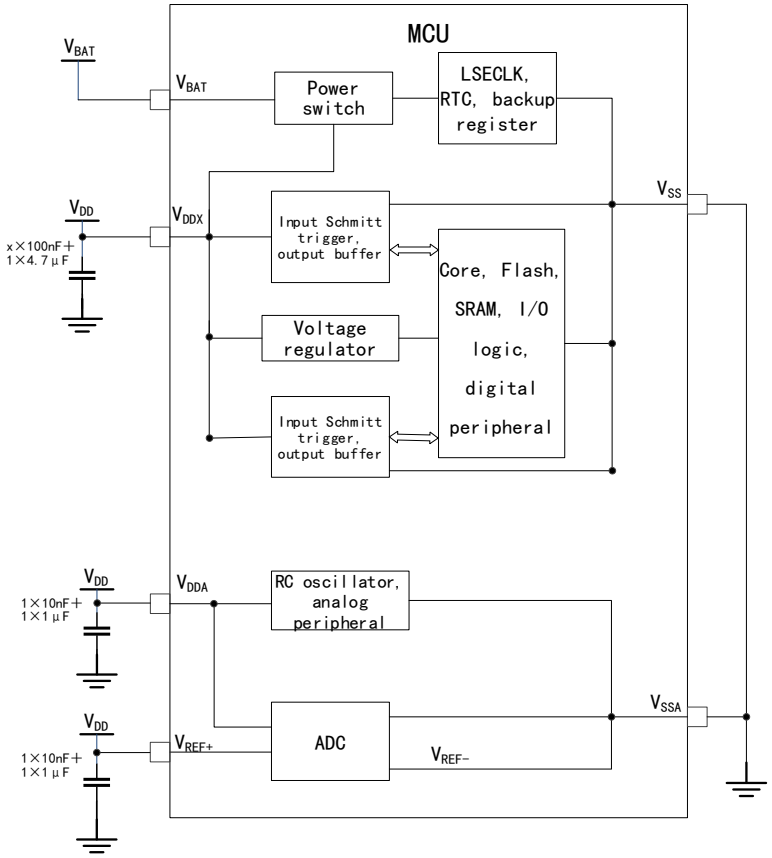
Unless otherwise specified, typical data are measured based on T_A=25℃, V_{DD}=V_{DDA}=3.3V. These data are only used for design guidance.

5.1.3 Typical curve

Unless otherwise specified, typical curves can only be used for design guidance and are not tested.

5.1.4 Power supply scheme

Figure 7 Power Supply Scheme



Notes: V_{DDx} in the figure means that the number of V_{DD} is x

5.1.5 Load capacitance

Figure 8 Load Conditions When Measuring Pin Parameters

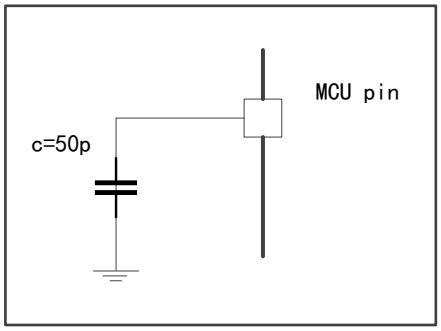


Figure 9 Pin Input Voltage Measurement Scheme

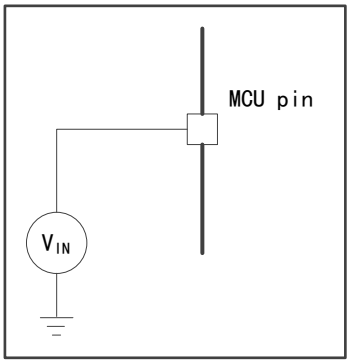
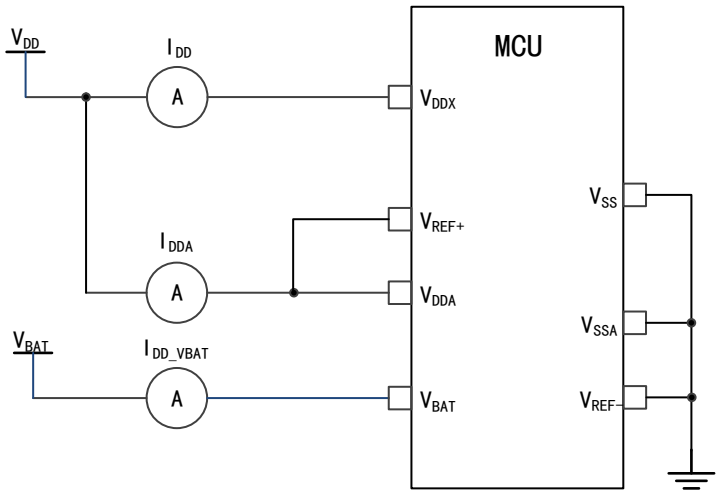


Figure 10 Power Consumption Measurement Scheme



5.2 Test under General Operating Conditions

Table 14 General Operating Conditions

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	120	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	-	60	
f_{PCLK2}	Internal APB2 clock frequency	-	-	120	
V_{DD}	Main power supply voltage	-	2	3.6	V
V_{DDA}	Analog power supply voltage (When ADC is not used)	It must be the same as V_{DD}	V_{DD}	3.6	V
	Analog power supply voltage (When ADC is used)		2.4	3.6	
V_{BAT}	Power supply voltage of backup domain	-	1.8	3.6	V
T_A	Ambient temperature (temperature number 6)	Maximum power dissipation	-40	85	℃
	Ambient temperature (temperature number 7)	Maximum power dissipation	-40	105	℃

Note: During power-on and normal operation, it is recommended to use the same power supply to power V_{DD} and V_{DDA}, with a maximum difference of 300mV between V_{DD} and V_{DDA}.

5.3 Absolute maximum rated value

If the load on the device exceeds the absolute maximum rated value, permanent damage may be caused to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

5.3.1 Maximum temperature characteristics

Table 15 Temperature Characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-55 ~ +150	℃
T_J	Maximum junction temperature	150	℃

5.3.2 Maximum rated voltage characteristics

All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the power supply within the external limited range.

Table 16 Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
V_{DD} - V_{SS}	External main power supply voltage	-0.3	4.0	V
V_{DDA}-V_{SSA}	External analog power supply voltage	-0.3	4.0	
V_{BAT}-V_{SS}	External backup power supply voltage	-0.3	4.0	
| V_{DD}-V_{DDA} |	Voltage difference allowed by V_{DD}>V_{DDA}	-	0.3	
V_{IN}	Input voltage on FT pins	V_{SS}-0.3	5.5	
	Input voltage on other pins	V_{SS}-0.3	V_{DD} + 0.3	
| ΔV_{DDx} |	Voltage difference between different power supply pins	-	50	mV
| V_{SSx}-V_{SS} |	Voltage difference between different grounding pins	-	50	

5.3.3 Maximum rated current characteristics

Table 17 Current Characteristics

Symbol	Description	Maximum value	Unit
I_{VDD}	Total current through V_{DD}/V_{DDA} power line (supply current) [1]	150	mA
I_{VSS}	Total current through V_{SS} ground line (outflow current) [1]	150	
I_{IO}	Sink current on any I/O and control pin	25	
	Source current on any I/O and control pin	-25	

Symbol	Description	Maximum value	Unit
$I_{INJ(PIN)}$[2]	Injection current of 5T pin[3]	-5/+0	
	Injection current of other pins[4]	±5	
$\Sigma I_{INJ(PIN)}$[2]	Total injection current on all I/O and control pins[5]	±25	

Note:

[1] All power supplies (VDD, VDDA) and ground (VSS, VSSA) must always be within the allowed range.

[2] The outflow current will interfere with the analog performance of the device.

[3] I/O cannot be injected positively: when VIN<VSS, IINJ(PIN) cannot exceed the maximum allowable input voltage value.

[4] If VIN exceeds the maximum value, IINJ(PIN) must be externally limited not to exceed the maximum value. When VIN> VDD, the current flows into the pins; when VIN<VSS, the current flows out of the pins.

[5] When the current is injected into several I/O ports at the same time, the maximum value of ΣIINJ(PIN) is the sum of instantaneous absolute value of inflow current and outflow current.

5.3.4 Electrostatic discharge (ESD)

Table 18 ESD Absolute Maximum Ratings

Symbol	Parameter	Condition	Value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A= +25℃	±5000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A=+25℃	±1000	V

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.3.5 Latch-up (LU)

Table 19 Static Latch-up

Symbol	Parameter	Condition	Type
LU	Latch-up class	T_A=25℃, conforming to EIA/JESD78E	Class Ⅰ A

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.4 Memory

5.4.1 Flash characteristics

Table 20 Flash Memory Characteristics[1]

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
tprog	16-bit programming time	T_A = -40~105℃ V_{DD}=2.0~3.6V	50	57	65	μs
t_{ERASE}	Page (1KBytes) erase time		3	-	4	ms
t_{ME}	Mass erase time		8	-	10	ms
V_{RET}	Data retention time	T_A = 105℃	10	-	-	years
N_{RW}	Erasure cycles	T_A = 105℃	100K	-	-	cycles

Note:[1] The data are obtained from a comprehensive evaluation and are not tested in production.

5.5 Clock

5.5.1 Characteristics of external clock source

High-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 21 Characteristics of HSECLK4~26MHz Oscillator [1]

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	V_{DD}=2.0~3.6V，T_A=-40~105℃	-	8	-	MHz
R_F	Feedback resistance	V_{DD}=3.3V，T_A=25℃	-	207	-	kΩ
i2	Drive current		-	1.16	-	mA
$I_{DD(HSECLK)}$	HSECLK current consumption		-	414	-	μA
$t_{SU(HSECLK)}$	Startup time	V_{DD}=2.0~3.6V，T_A=-40~105℃	-	0.75	-	ms
$DuCy_{(HSECLK)}$	Duty cycle		-	50	-	%

Note: [1] The data are obtained from a comprehensive evaluation and are not tested in production.

Low-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 22 Characteristics OF LSECLK Oscillator (f_{LSECLK}=32.768kHz)[1]

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	V_{DD}=2.0~3.6V，T_A=-40~105℃	-	32.762	-	KHz
R_F	Feedback resistance	V_{DD}=3.3V，T_A=25℃	-	3.78	-	MΩ
i2	Drive current		-	0.38	-	μA
$I_{DD(LSECLK)}$	LSECLK current consumption		-	1.17	-	μA
$t_{SU(LSECLK)}$[2]	Startup time	V_{DD}=2.0~3.6V，T_A=-40~105℃	-	1.60	-	s
$DuCy_{(LSECLK)}$	Duty cycle		-	51.94	-	%

Note:

[1] The data are obtained from a comprehensive evaluation and are not tested in production.

[2] $t_{SU(LSECLK)}$ is the startup time, which is measured from the time when LSECLK is enabled by software to the time when stable oscillation at 32.768kHz is obtained. This value is measured using a standard crystal resonator, which may vary greatly due to different crystal manufacturers.

5.5.2 Characteristics of internal clock source

High-speed internal (HSICLK) RC oscillator

Table 23 Characteristics of HSICLK Oscillator[1]

Symbol	Parameter	Condition		Minimum value	Typical value	Maximum value	Unit
f_{HSICLK}	Frequency	V_{DD}=2.0~3.6V，T_A=-40~105℃		-	8	-	MHz
$DuCy_{(HSICLK)}$	Duty cycle			-	52.46	-	%
$A_{CC(HSICLK)}$	Accuracy of HSICLK oscillator	Factory calibration	-1	-	1	%	%
			-2.5	-	2.5	%	%
$I_{DDA(HSICLK)}$	Power consumption of HSICLK oscillator	V_{DD}=3.3V，T_A=25℃		-	127	-	μA
$t_{SU(HSICLK)}$	Startup time of HSICLK oscillator	V_{DD}=2.0~3.6V, T_A=-40~105℃		-	1.52	-	μs

Note: [1] The data are obtained from a comprehensive evaluation and are not tested in production.

Low-speed internal (LSICLK) RC oscillator

Table 24 Characteristics of LSICLK Oscillator[1]

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{LSICLK}	Frequency	V_{DD}=2.0-3.6V，T_A=-40~105℃	-	44.97	-	kHz
$I_{DD(LSICLK)}$	Power consumption of LSICLK oscillator	3.3V/25℃	-	1.09	-	μA
$t_{SU(LSICLK)}$	Startup time of LSICLK oscillator	V_{DD}=2.0-3.6V，T_A=-40~105℃	-	80.1	-	μs
$DuCy_{(HSICLK)}$	Duty cycle		-	49.92	-	%

Note:[1]The data are obtained from a comprehensive evaluation and are not tested in production.

5.5.3 PLL characteristics

Table 25 PLL Characteristics[1]

Symbol	Parameter	Value			Unit
		Minimum value	Typical value	Maximum value	
f_{PLL_IN}	PLL input clock	-	8	-	MHz
	Duty cycle of PLL input clock	-	60.19	-	%
t_{LOCK}	PLL phase locking time	-	131	-	μs
-	Commonly used frequency doubling and jitter	-	1955	-	ps

Note:[1]The data are obtained from a comprehensive evaluation and are not tested in production.

5.6 Power supply and power supply management

5.6.1 Power-on/power-down characteristics

Table 26 Power-on/power-down Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{VDD}	V_{DD} rise time rate	-	10	-	200000	μs/V
	V_{DD} fall time rate		10	-	200000	

5.6.2 Test of embedded reset and power control module characteristics

Table 27 Embedded Reset and Power Control Module Characteristics[1]

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{POR}	Power-on reset threshold	V_{DD}=3.3V，T_A=-40~105℃	1.84	1.845	1.85	V
V_{PDR}	power-down reset threshold		1.79	1.795	1.80	V
$V_{PDRhyst}$	PDR hysteresis		40	50	60	mV
$T_{RSTTEMPO}$	Reset duration		0.96	1.28	1.52	ms

Note:[1]The data are obtained from a comprehensive evaluation and are not tested in production.

Table 28 Programmable Power Supply Voltage Detector Characteristics[1]

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{PVD}	Programmable power supply voltage detector voltage level selection	PLS[2:0]=000 (rising edge)	2.15	-	2.17	V
		PLS[2:0]=000 (falling edge)	2.05	-	2.07	V
		PLS[2:0]=001 (rising edge)	2.25	-	2.27	V
		PLS[2:0]=001 (falling edge)	2.14	-	2.16	V
		PLS[2:0]=010 (rising edge)	2.35	-	2.37	V
		PLS[2:0]=010 (falling edge)	2.24	-	2.26	V
		PLS[2:0]=011 (rising edge)	2.44	-	2.46	V
		PLS[2:0]=011 (falling edge)	2.34	-	2.36	V
		PLS[2:0]=100 (rising edge)	2.54	-	2.56	V
		PLS[2:0]=100 (falling edge)	2.43	-	2.45	V
		PLS[2:0]=101 (rising edge)	2.63	-	2.66	V
		PLS[2:0]=101 (falling edge)	2.53	-	2.55	V
		PLS[2:0]=110 (rising edge)	2.73	-	2.76	V
		PLS[2:0]=110 (falling edge)	2.62	-	2.65	V

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
		PLS[2:0]=111 (rising edge)	2.84	-	2.87	V
		PLS[2:0]=111 (falling edge)	2.72	-	2.75	V

Note: [1]The data are obtained from a comprehensive evaluation and are not tested in production.

5.7 Power Consumption

5.7.1 Power consumption test environment

(1) The values are measured by executing Dhrystone 2.1, with the Keil.V5 compilation environment and the L0 compilation optimization level.

(2) All I/O pins are in input mode and are connected to a static level at V_{DD} or V_{SS} (no load).

(3) Unless otherwise specified, all peripherals are disabled.

(4) The relationship between Flash wait cycle setting and f_{HCLK}:

0~30MHz: 0 wait cycle

30~60MHz: 1 wait cycle

60~90MHz: 2 wait cycles

90~120MHz: 3 wait cycles

The wait cycle of Flash is different, and the power consumption will increase during operation if the programs are placed in Flash

(5) The instruction prefetch function is enabled (Note: it must be set before clock setting and bus frequency division).

(6) When the peripherals are enabled: $f_{PCLK1}=f_{HCLK}/2$，$f_{PCLK2}=f_{HCLK}$

5.7.2 Power consumption in operation mode

Table 29 Power Consumption in Run Mode when the Program is Executed in Flash (FACC Enabled)[1]

Parameter	Condition	f_{HCLK}	Typical value	Maximum value	Unit
			T_A=25℃, V_{DD}=3.3V	T_A=105℃, V_{DD}=3.6V	
Power consumption in operation mode	HSECLK bypass[2], enabling all peripherals	120MHz	15.05	17.43	mA
		96MHz	12.12	14.03	
		72MHz	9.85	11.38	
		48MHz	7.47	8.97	
		36MHz	5.89	7.35	
		24MHz	4.66	6.13	
		16MHz	3.56	5.01	
		8MHz	2.47	3.95	
	HSECLK bypass[2], disabling all peripherals	120MHz	9.55	11.01	
		96MHz	7.95	9.42	
		72MHz	6.57	8.02	

Parameter	Condition	f_{HCLK}	Typical value	Maximum value	Unit
			T_A=25℃, V_{DD}=3.3V	T_A=105℃, V_{DD}=3.6V	
		48MHz	4.95	6.40	
		36MHz	3.99	5.34	
		24MHz	3.26	4.57	
		16MHz	.2.58	3.66	
		8MHz	1.91	3.00	
	HSICLK[2], enabling all peripherals	64MHz	10.75	12.04	
		48MHz	8.41	9.81	
		32MHz	6.49	7.87	
		24MHz	4.53	5.90	
		16MHz	3.37	4.77	
		8MHz	2.15	3.58	
	HSICLK[2], disabling all peripherals	64MHz	4.90	6.20	
		48MHz	3.75	4.97	
		32MHz	2.91	4.15	
		24MHz	2.18	3.33	
		16MHz	1.75	2.81	
		8MHz	1.30	2.39	

Note:

[1] The data are obtained from a comprehensive evaluation and are not tested in production.

[2] The external clock is 8MHz. When f_{HCLK}>8MHz, PLL is enabled; otherwise, PLL is disabled.

Table 30 Power Consumption in Run Mode when the Program is Executed in Flash (FACC Disabled)[1]

Parameter	Condition	f_{HCLK}	Typical value	Maximum value	Unit
			T_A=25℃, V_{DD}=3.3V	T_A=105℃, V_{DD}=3.6V	
Power consumption in operation mode	HSECLK bypass[2], enabling all peripherals	120MHz	15.26	17.09	mA
		96MHz	12.57	14.01	
		72MHz	10.33	11.79	
		48MHz	7.95	9.26	
		36MHz	6.37	7.52	
		24MHz	5.28	6.66	
		16MHz	4.17	5.78	
		8MHz	2.96	4.01	

Parameter	Condition	f_{HCLK}	Typical value	Maximum value	Unit
			T_A=25℃, V_{DD}=3.3V	T_A=105℃, V_{DD}=3.6V	
	HSECLK bypass[2], disabling all peripherals	120MHz	10.04	11.54	
		96MHz	8.41	9.96	
		72MHz	7.00	8.52	
		48MHz	5.40	6.88	
		36MHz	4.46	5.87	
		24MHz	3.71	4.96	
		16MHz	3.04	4.12	
		8MHz	2.36	3.46	
	HSICLK[2], enabling all peripherals	64MHz	10.73	12.11	
		48MHz	8.35	9.73	
		32MHz	6.47	7.78	
		24MHz	4.52	5.83	
		16MHz	3.35	4.77	
		8MHz	2.15	3.58	
	HSICLK[2], disabling all peripherals	64MHz	4.89	6.16	
		48MHz	3.76	5.01	
		32MHz	2.91	4.18	
		24MHz	2.18	3.37	
		16MHz	1.75	2.81	
		8MHz	1.29	2.39	

Note:

[1] The data are obtained from a comprehensive evaluation and are not tested in production.

[2] The external clock is 8MHz. When f_{HCLK}>8MHz, PLL is enabled; otherwise, PLL is disabled.

Table 31 Power Consumption in Run Mode when the Program is Executed in RAM[1]

Parameter	Condition	f_{HCLK}	Typical value	Maximum value	Unit
			T_A=25℃, V_{DD}=3.3V	T_A=105℃, V_{DD}=3.6V	
Power consumption in operation mode	HSECLK bypass[2], enabling all peripherals	120MHz	17.41	18.89	mA
		96MHz	14.23	15.69	
		72MHz	11.17	13.04	
		48MHz	8.12	9.56	
		36MHz	6.43	7.85	

Parameter	Condition	f_{HCLK}	Typical value	Maximum value	Unit
			T_A=25℃, V_{DD}=3.3V	T_A=105℃, V_{DD}=3.6V	
		24MHz	4.88	6.15	
		16MHz	3.85	5.05	
		8MHz	2.83	4.01	
	HSECLK bypass[2], disabling all peripherals	120MHz	9.79	11.15	
		96MHz	8.17	9.59	
		72MHz	6.48	7.82	
		48MHz	4.78	6.18	
		36MHz	3.99	5.23	
		24MHz	3.27	4.47	
		16MHz	2.74	3.80	
		8MHz	2.20	3.30	
	HSICLK[2], enabling all peripherals	64MHz	9.51	12.24	
		48MHz	7.32	8.48	
		32MHz	5.59	6.93	
		24MHz	4.04	5.14	
		16MHz	2.97	4.09	
		8MHz	1.93	3.09	
	HSICLK[2], disabling all peripherals	64MHz	5.01	6.27	
		48MHz	3.91	5.13	
		32MHz	3.09	4.24	
		24MHz	2.30	3.28	
		16MHz	1.83	2.89	
		8MHz	1.30	2.33	

Note:

[1] The data are obtained from a comprehensive evaluation and are not tested in production.

[2] The external clock is 8MHz. When f_{HCLK}>8MHz, PLL is enabled; otherwise, PLL is disabled.

5.7.3 Power consumption in sleep mode

Table 32 Power Consumption in Sleep Mode when the Program is Executed in Flash(FACC Enabled) [1]

Parameter	Condition	f_{HCLK}	Typical value	Maximum value	Unit
			T_A=25℃, V_{DD}=3.3V	T_A=105℃, V_{DD}=3.6V	
		120MHz	11.60	13.29	mA

Parameter	Condition	f_{HCLK}	Typical value	Maximum value	Unit
			T_A=25℃, V_{DD}=3.3V	T_A=105℃, V_{DD}=3.6V	
Power consumption in sleep mode	HSECLK bypass[2], enabling all peripherals	96MHz	9.53	11.19	
		72MHz	7.50	9.09	
		48MHz	5.48	6.86	
		36MHz	4.37	5.86	
		24MHz	3.38	4.67	
		16MHz	2.71	4.16	
		8MHz	2.04	3.52	
	HSECLK bypass[2], disabling all peripherals	120MHz	3.50	4.80	
		96MHz	3.20	4.43	
		72MHz	2.78	3.95	
		48MHz	2.37	3.56	
		36MHz	1.96	3.17	
		24MHz	1.76	2.85	
		16MHz	1.62	2.80	
		8MHz	1.48	2.60	
	HSICLK[2], enabling all peripherals	64MHz	6.44	7.60	
		48MHz	5.06	6.47	
		32MHz	3.94	5.34	
		24MHz	2.90	4.11	
		16MHz	2.27	3.70	
		8MHz	1.60	3.03	
	HSICLK[2], disabling all peripherals	64MHz	1.80	2.97	
		48MHz	1.51	2.62	
		32MHz	1.32	2.39	
		24MHz	1.13	2.19	
		16MHz	1.04	2.11	
		8MHz	0.90	1.99	

Note:

[1] The data are obtained from a comprehensive evaluation and are not tested in production.

[2] The external clock is 8MHz. When f_{HCLK}>8MHz, PLL is enabled; otherwise, PLL is disabled.

Table 33 Power Consumption in Sleep Mode when the Program is Executed in Flash(FACC Disabled) [1]

Parameter	Condition	f_{HCLK}	Typical value	Maximum value	Unit
			T_A=25℃, V_{DD}=3.3V	T_A=105℃, V_{DD}=3.6V	
Power consumption in sleep mode	HSECLK bypass[2], enabling all peripherals	120MHz	12.06	13.46	mA
		96MHz	10.00	11.88	
		72MHz	7.98	9.56	
		48MHz	5.92	7.30	
		36MHz	4.81	6.12	
		24MHz	3.93	5.08	
		16MHz	3.16	4.32	
		8MHz	2.48	3.77	
	HSECLK bypass[2], disabling all peripherals	120MHz	1.34	2.45	
		96MHz	3.66	4.90	
		72MHz	3.24	4.47	
		48MHz	2.82	4.04	
		36MHz	2.41	3.62	
		24MHz	2.22	3.40	
		16MHz	2.08	3.25	
		8MHz	1.93	3.13	
	HSICLK[2], enabling all peripherals	64MHz	6.40	7.65	
		48MHz	5.04	6.47	
		32MHz	3.94	5.29	
		24MHz	2.89	4.14	
		16MHz	2.27	3.70	
		8MHz	1.60	3.06	
	HSICLK[2], disabling all peripherals	64MHz	1.80	2.97	
		48MHz	1.51	2.62	
		32MHz	1.32	2.39	
		24MHz	1.13	2.19	
		16MHz	1.04	2.11	
		8MHz	0.90	2.00	

Note:

[1] The data are obtained from a comprehensive evaluation and are not tested in production.

[2] The external clock is 8MHz. When f_{HCLK}>8MHz, PLL is enabled; otherwise, PLL is disabled.

Table 34 Power Consumption in Sleep Mode when the Program is Executed in RAM[1]

Parameter	Condition	f_{HCLK}	Typical value	Maximum value	Unit
			T_A=25℃, V_{DD}=3.3V	T_A=105℃, V_{DD}=3.6V	
Power consumption in sleep mode	HSECLK bypass[2], enabling all peripherals	120MHz	12.09	13.52	mA
		96MHz	10.04	11.42	
		72MHz	7.98	9.59	
		48MHz	5.92	7.27	
		36MHz	4.80	6.08	
		24MHz	3.83	5.11	
		16MHz	3.14	4.32	
		8MHz	2.46	3.65	
	HSECLK bypass[2], disabling all peripherals	120MHz	3.64	4.84	
		96MHz	3.24	4.47	
		72MHz	2.83	4.01	
		48MHz	2.41	3.58	
		36MHz	2.21	3.34	
		24MHz	2.07	3.16	
		16MHz	1.93	3.04	
		8MHz	1.79	2.88	
	HSICLK[2], enabling all peripherals	64MHz	6.69	9.31	
		48MHz	5.15	6.33	
		32MHz	3.95	5.16	
		24MHz	2.98	4.14	
		16MHz	2.27	3.39	
		8MHz	1.58	2.79	
	HSICLK[2], disabling all peripherals	64MHz	1.78	2.94	
		48MHz	1.51	2.66	
		32MHz	1.30	2.33	
		24MHz	1.11	2.13	
		16MHz	1.02	2.05	
		8MHz	0.89	1.96	

Note:

[1] The data are obtained from a comprehensive evaluation and are not tested in production.

[2] The external clock is 8MHz. When f_{HCLK}>8MHz, PLL is enabled; otherwise, PLL is disabled.

5.7.4 Power consumption in stop and sleep modes

Table 35 Power Consumption in Stop and Standby Modes[1]

Parameter	Condition	Typical value, (T_A=25℃, V_{DD}=3.3V)	Unit
Power consumption in stop mode	Voltage regulator in operation mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	97.73	μA
	Voltage regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog)	86.36	
Power consumption in standby mode	Low-speed internal RC oscillator and independent watchdog ON	3.30	
	Low-speed internal RC oscillator on, independent watchdog OFF	3.14	
	Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	3.10	

Note: [1] The data are obtained from a comprehensive evaluation and are not tested in production.

5.7.5 Backup domain power consumption

Table 36 Backup Domain Power Consumption[1]

Symbol	Condition	Typical value, T_A=25℃, V_{BAT}=3.3V	Unit
I_{DD_VBAT}	Low-speed oscillator and RTC ON	1.75	μA

Note: [1] The data are obtained from a comprehensive evaluation and are not tested in production.

5.7.6 Peripheral power consumption

The HSECLK Bypass 1M is adopted as clock source, f_{PCLK}=f_{HCLK}=1M.

Peripheral power consumption = current that enables the peripheral clock - current that disables the peripheral clock.

Table 37 Peripheral Power Consumption[1]

Parameter	Peripheral	Typical value T_A=25℃, V_{DD}=3.3V	Unit
AHB	DMA1	0.31	mA
	DMA2	0.28	mA
	CRC	0.02	mA
	USB OTG FS	2.01	mA
APB1	TMR2	0.45	mA
	TMR3	0.36	mA
	TMR4	0.35	mA

Parameter	Peripheral	Typical value T_A=25℃, V_{DD}=3.3V	Unit
	TMR5	0.35	mA
	WWDT	0.04	mA
	IWDT	0.04	mA
	SPI2/I2S	0.19	mA
	USART2	0.14	mA
	USART3	0.14	mA
	UART4	0.12	mA
	I2C1	0.11	mA
	CAN1	0.18	mA
	CAN2	0.17	mA
	BAKPR	0.04	mA
	PMU	0.01	mA
APB2	GPIOA	0.20	mA
	GPIOB	0.20	mA
	GPIOC	0.19	mA
	GPIOD	0.17	mA
	ADC1	0.47	mA
	ADC2	0.44	mA
	TMR1	0.53	mA
	TMR8	0.54	mA
	SPI1	0.29	mA
	USART1	0.28	mA

Note: [1] The data are obtained from a comprehensive evaluation and are not tested in production.

5.8 Wake-up time in low-power mode

The measurement of wake-up time in low-power mode is from the start of wake-up event to the time when the user program reads the first instruction, in which V_{DD}=V_{DDA}.

Table 38 Wake-up Time in Low-power Mode[1]

Symbol	Parameter	Condition	Typical value (T_A=25℃,V_{DD}=3.3V)	Unit
$t_{WUSLEEP}$	Wake up from sleep mode	-	0.41	μs
t_{WUSTOP}	Wake up from stop mode	The voltage regulator is in run mode	22.7	

Symbol	Parameter	Condition	Typical value (T_A=25℃,V_{DD}=3.3V)	Unit
		The voltage regulator is in low-power mode	23.75	
$t_{WUSTDBY}$	Wake up from standby mode	-	80.72	

Note: [1] The data are obtained from a comprehensive evaluation and are not tested in production.

5.9 Pin characteristics

5.9.1 Characteristics of I/O pins

Table 39 DC Characteristics (Test Conditions V_{DD}=2.7~3.6V, T_A=-40~105℃)[1]

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
VIL	Low-level input voltage	CMOS port	-	-	0.3*V_{DD}	V
V_{IH}	High-level input voltage		0.7*V_{DD}	-	-	
VIL	Low-level input voltage	TTL port	-	-	0.8	
V_{IH}	High-level input voltage		2.0	-	-	
V_{hys}	Standard/5V FT I/O pin Schmitt trigger voltage hysteresis	CMOS port	0.1*V_{DD}	-	-	mV
		TTL port	200	-	-	mV
I_{lkg}	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/O port	-1	-	1	μA
		VIN=5V, FT port	-3	-	3	
R_{PU}	Weak pull-up equivalent resistance	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistance	V_{IN}=V_{DD}	30	40	50	kΩ

Note:[1] The data are obtained from a comprehensive evaluation and are not tested in production.

Table 40 AC Characteristics[1]

MODEy[1:0] Configuration [2]	Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
10 (2MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=50 pF, V_{DD}=2~3.6V	-	2	MHz
	$t_{f(IO)out}$	Fall time of output from high to low level	C_L=50 pF, V_{DD} =2~3.6V	-	125	ns
	$t_{r(IO)out}$	Rise time of output from low to high level		-	125	
01 (10MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=50 pF, V_{DD} =2~3.6V	-	10	MHz

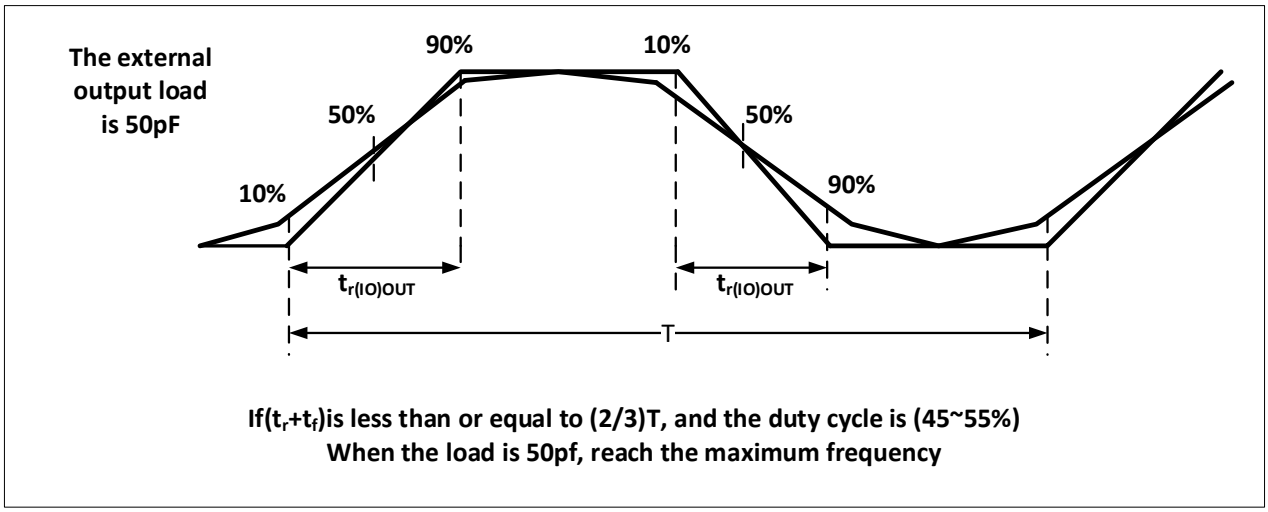
MODEy[1:0] Configuration [2]	Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
	$t_{f(IO)out}$	Fall time of output from high to low level	C_L=50 pF, V_{DD} =2~3.6V	-	25	ns
	$t_{r(IO)out}$	Rise time of output from low to high level		-	25	
11 (50MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=30 pF, V_{DD} =2.7~3.6V	-	50	MHz
	$t_{f(IO)out}$	Fall time of output from high to low level	C_L=30 pF, V_{DD} =2.7~3.6V	-	10	ns
	$t_{r(IO)out}$	Rise time of output from low to high level		-	10	

Note:

[1] The data are obtained from a comprehensive evaluation and are not tested in production.

[2] The speed of I/O port can be configured through MODEy.

Figure 11 I/O AC Characteristics Definition[1]



Note:[1] The data are obtained from a comprehensive evaluation and are not tested in production.

Table 41 Characteristics of Output Drive Current (Test Conditions V_{DD}=2.7~3.6V, T_A=-40~105℃)

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
V_{OL}	Output low level when 8 pins absorb/output current at the same time	I_{IO} = +8mA 2.7V<V_{DD}<3.6V	-	0.4	V
V_{OH}	Output high level when 8 pins absorb/output current at the same time		V_{DD}-0.4	-	
V_{OL}	Output low level when 8 pins absorb/output current at the same time	IIO = +20mA 2.7V<V_{DD}<3.6V	-	1.3	V
V_{OH}	Output high level when 8 pins absorb/output current at the same time		V_{DD}-1.3	-	

5.9.2 NRST pin characteristics

CMOS process is adopted for the NRST pin input drive, which is connected to a permanent pull-up resistor R_{PU} .

Table 42 Characteristics of NRST Pin (Test Conditions V_{DD}=3.3V, T_A=-40~105℃)[1]

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$V_{IL(NRST)}$	NRST low-level input voltage	-	-0.5	-	0.8	V
$V_{IH(NRST)}$	NRST high-level input voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistance	V_{IN} = V_{SS}	30	40	50	kΩ

Note: [1] The data are obtained from a comprehensive evaluation and are not tested in production.

5.10 Communication peripherals

5.10.1 I2C peripheral characteristics

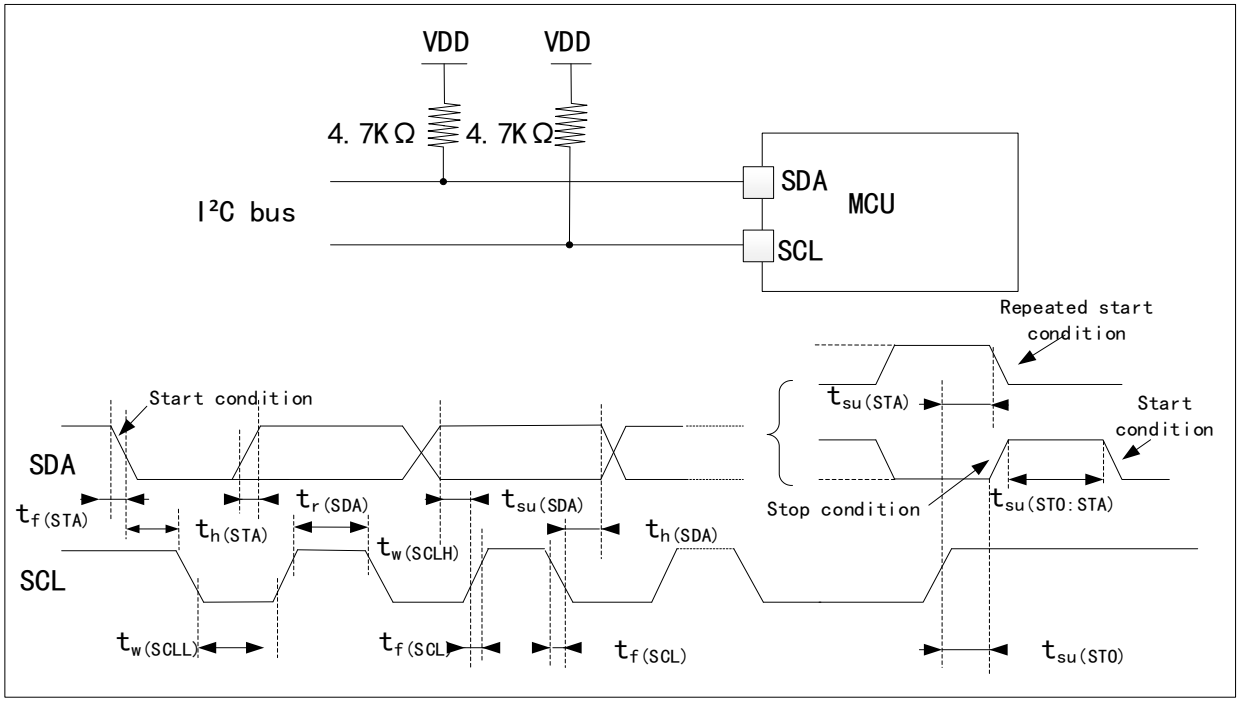
To achieve the maximum frequency of I2C in standard mode, f_{PCLK1} must be greater than 2MHz. To achieve maximum frequency of I2C in fast mode, f_{PCLK1} must be greater than 4MHz.

Table 43 I2C Interface Characteristics (T_A=25℃, V_{DD}=3.3V) [1]

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Minimum value	Maximum value	Minimum value	Maximum value	
$t_{w(SCLL)}$	SCL clock low time	5.05	-	1.7	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.9	-	0.77	-	
$t_{su(SDA)}$	SDA setup time	4422	-	1105	-	ns
$t_{h(SDA)}$	SDA data hold time	-	468	-	477	
$t_{r(SDA)}$/$t_{r(SCL)}$	SDA and SCL rise time	-	169.5	-	168.3	
$t_{f(SDA)}$/$t_{f(SCL)}$	SDA and SCL fall time	-	7.09	-	7.39	
$t_{h(STA)}$	Start condition hold time	5.0	-	0.83	-	μs
$t_{su(STA)}$	Setup time of repeated start condition	4.97	-	0.83	-	
$t_{su(STO)}$	Setup time of stop condition	5.0	-	0.82	-	
$t_{w(STO:STA)}$	Time from stop condition to start condition (the bus is idle)	5.3	-	2.02	-	

Note:[1] The data are obtained from a comprehensive evaluation and are not tested in production.

Figure 12 Bus AC Waveform and Measurement Circuit



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.10.2 SPI peripheral characteristics

Table 44 SPI Characteristics (T_A=25℃, V_{DD}=3.3V) [1]

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SP clock rise and fall time	Load capacitance: C = 30pF	-	4.9	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	90	121	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	69	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36MHz, Prescaler factor=4	50	60	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	50	-	ns
		Slave mode	50	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	34	-	ns
		Slave mode	27	-	
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK}= 20MHz	5	7	ns
$t_{dis(SO)}$	Disable time of data output	Slave mode	14	18	ns

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
$t_{v(SO)}$	Effective time of data output	Slave mode (after enabling the edge)	7.4	10.8	ns
$t_{v(MO)}$	Effective time of data output	Master mode (after enabling the edge）	2.4	5.5	ns
$t_{h(SO)}$	Data output hold time	Slave mode （after enabling the edge）	8	11	ns
$t_{h(MO)}$		Master mode (after enabling the edge）	1	1.7	

Note: [1]The data are obtained from a comprehensive evaluation and are not tested in production.

Figure 13 SPI Timing Diagram - Slave Mode and CPHA=0

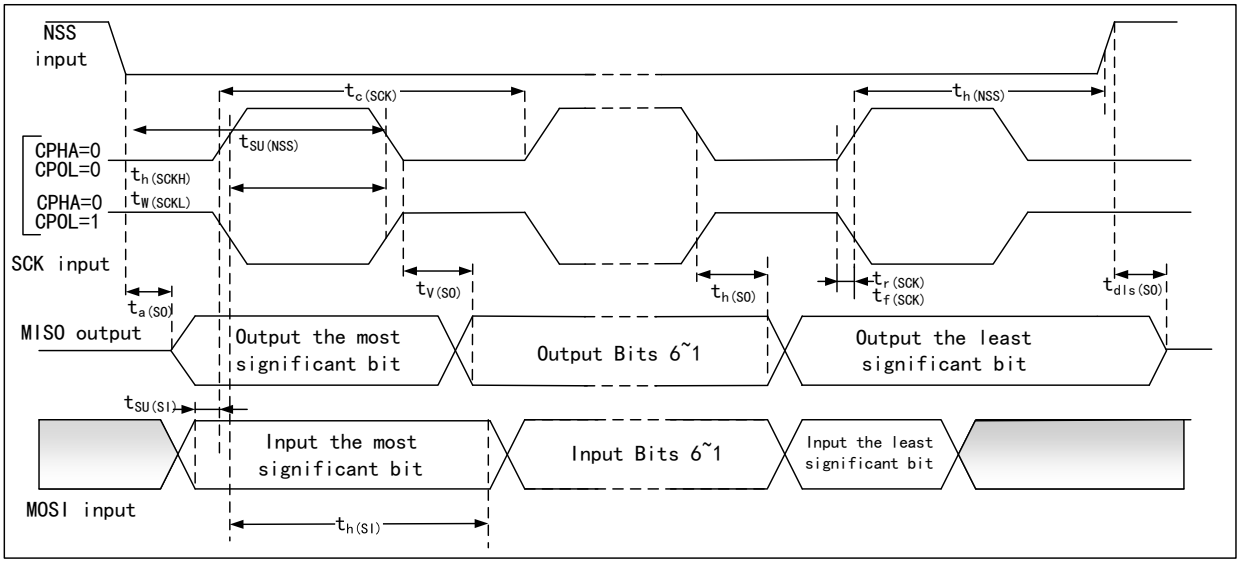
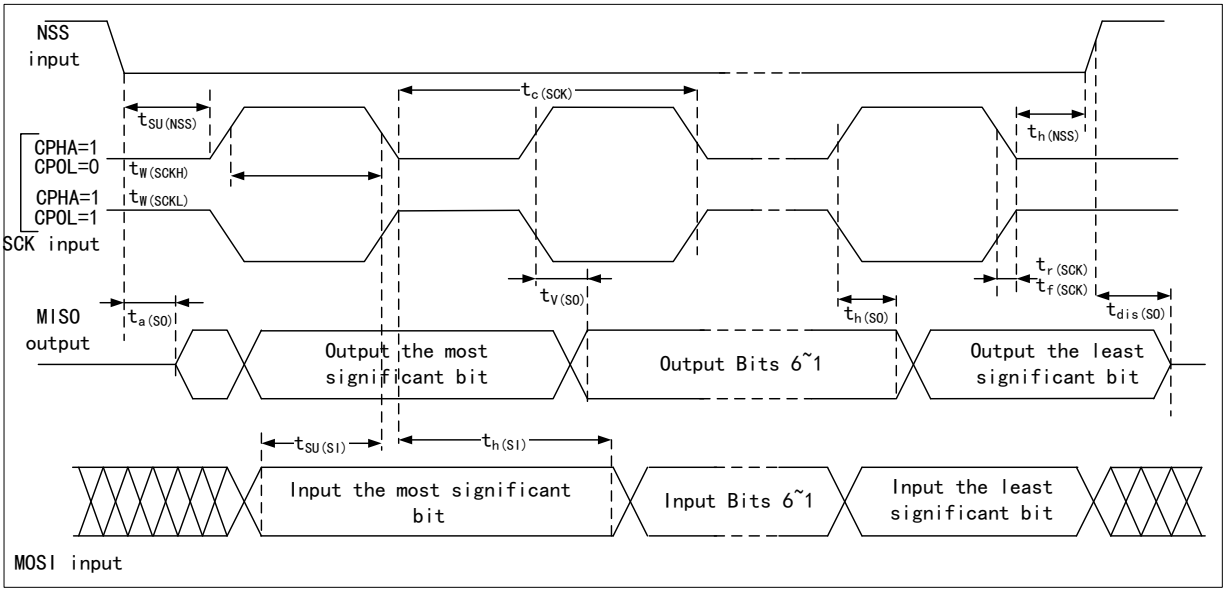
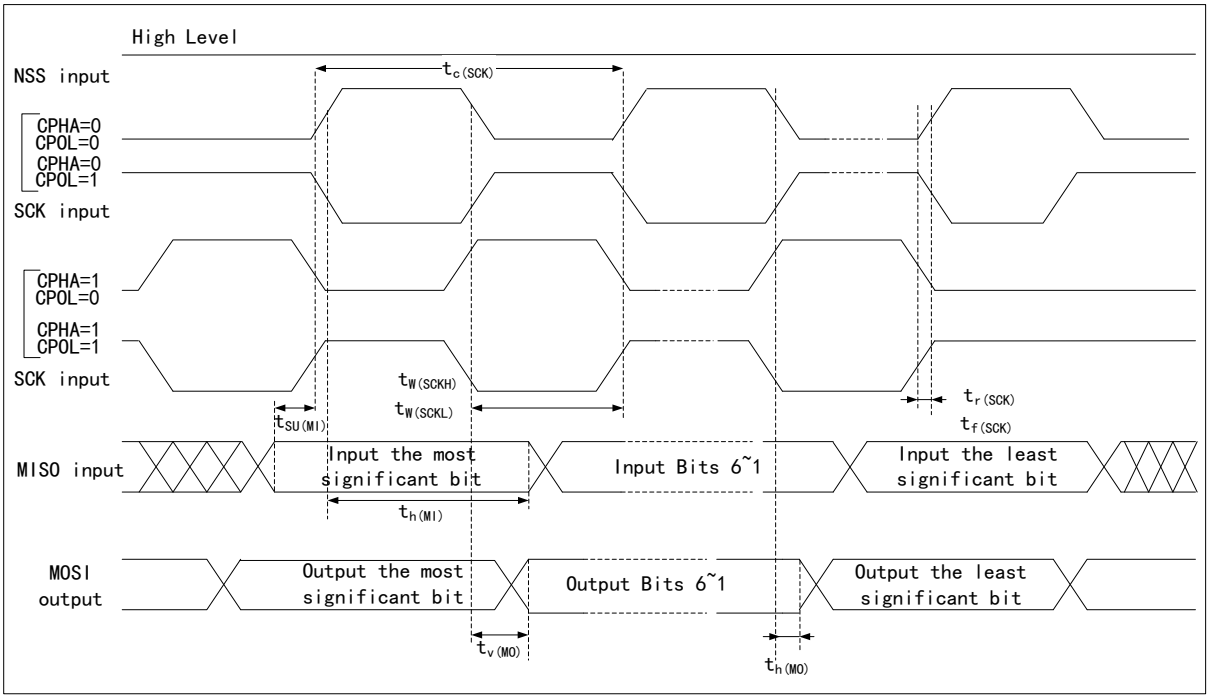


Figure 14 SPI Timing Diagram - Slave Mode and CPHA=1



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 15 SPI Timing Diagram - Master Mode



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.11 Analog peripherals

5.11.1 ADC

Test parameter description:

- Sampling rate: The number of times of conversion from analog to digital quantity per second by ADC; sampling rate=ADC clock/(number of sampling cycles+number of conversion cycles)

5.11.1.1 12-bit ADC characteristics

Table 45 12-bit ADC Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{DDA}	Supply voltage	-	2.4	-	3.6	V
I_{DDA}	ADC power consumption	V_{DDA}=3.3V, f_{ADC}=14MHz, Sampling time=1.5 f_{ADC}	1.06	-	1.14	mA
f_{ADC}	ADC frequency	-	0.6	-	14	MHz
C_{ADC}	Internal sampling and holding capacitance	-	-	8	-	pF
R_{ADC}	Sampling resistor	-	-	-	1000	Ω
t_S	Sampling time	f_{ADC}=14MHz	0.107	-	17.1	μs

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
T_{CONV}	Sampling and conversion time	f_{ADC}=14MHz, 12-bit conversion	1.3	-	18.32	μs

Table 46 12-bit ADC Accuracy[1]

Symbol	Parameter	Condition	Typical value	Maximum value	Unit
E_T	Composite error	f_{PCLK}=56MHz, f_{ADC}=14MHz, V_{DDA}=2.4V-3.6V T_A=-40℃~105℃	-1.37	2.93	LSB
E_O	Offset error		-0.4	1.43	
E_G	Gain error		-0.47	1.87	
E_D	Differential linear error		-1.02	1.07	
E_L	Integral linear error		-2.4	2	

Note: [1] The data are obtained from a comprehensive evaluation and are not tested in production.

5.11.1.2 Temperature sensor characteristics

Table 47 Characteristics of Temperature Sensor

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
Slope[1]	Average slope (V_{DD} = 3.3V, T_A = -40~85℃)	-	4.0	-	mV/ºC
V25	Voltage at 25ºC (V_{DD}= 3.3V)	-	1.46	-	V
TS_temp[2]	ADC sampling time when reading the temperature	10	-	-	μs

Note:

[1] Guaranteed by design and not tested in production.

[2] The minimum sampling time can be determined by multiple loops in the application.

5.11.1.3 Test of Built-in Reference Voltage Characteristics

Table 48 Built-in Reference Voltage Characteristics[1]

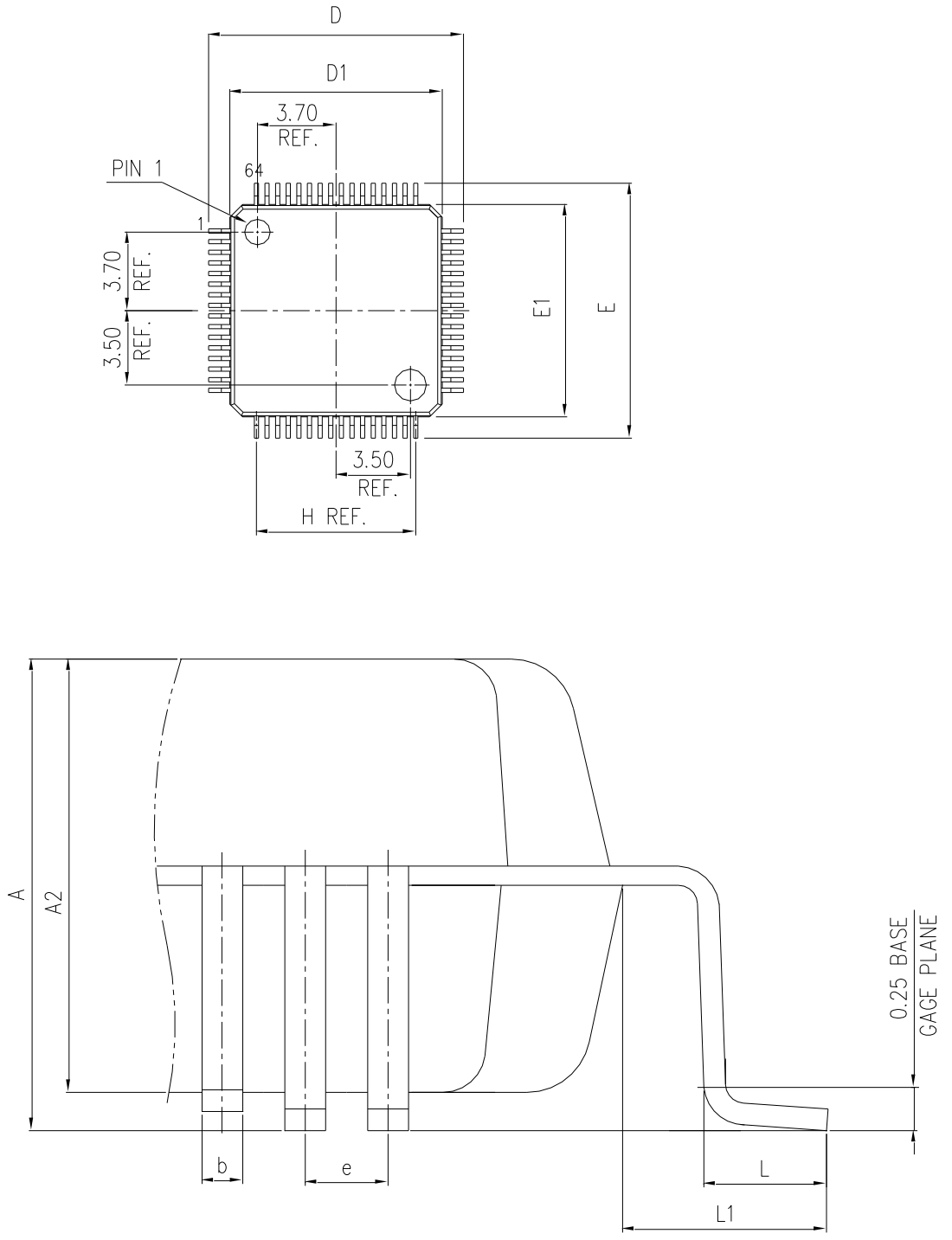
Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{REFINT}	Built-in reference voltage	-40℃ < T_A < +105℃ V_{DD}= 2-3.6 V	1.1882	1.1947	1.2002	V
$T_{S\_vrefint}$	Sampling time of ADC when reading out internal reference voltage	-	-	5.1	17.1	μs
V_{RERINT}	Built-in reference voltage extends to temperature range	V_{DD}=3V ±10mV	-	-	18	mV
T_{coeff}	Temperature coefficient	-	-	-	104	ppm/℃

Note: [1] The data are obtained from a comprehensive evaluation and are not tested in production.

6 Package Information

6.1 LQFP64 Package Diagram

Figure 16 LQFP64 Package Diagram



Note:

(1) The figure is not drawn to scale.

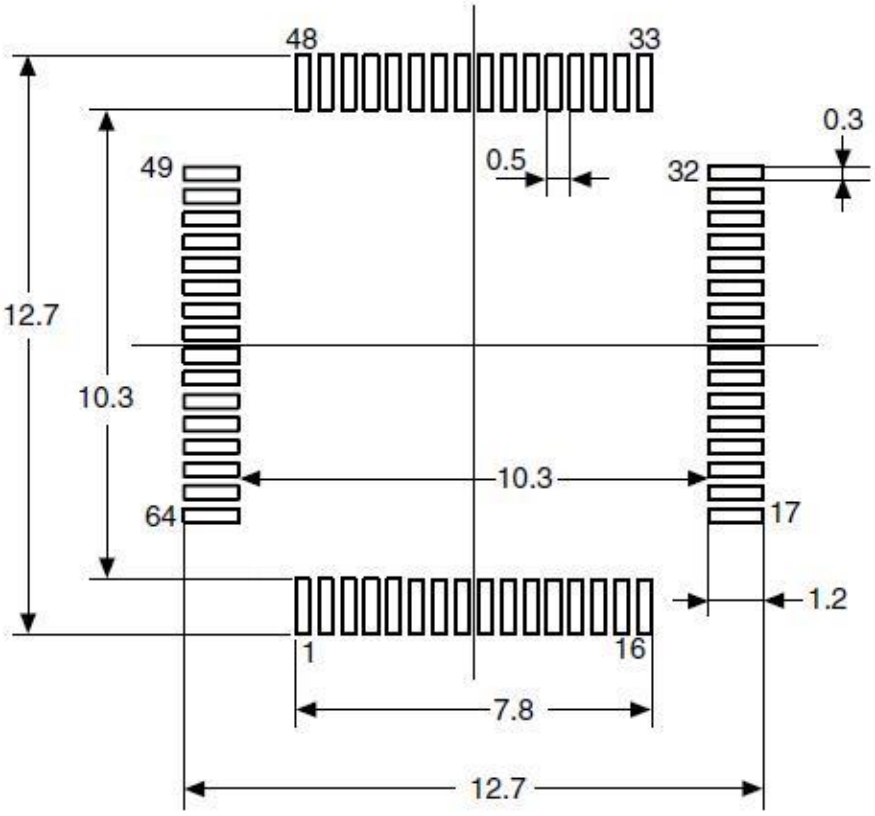
(2) All pins should be soldered to the PCB.

49Table LQFP64 Package Data

DIMENSION LIST（FOOTPRINT: 2.00）			
S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	12.000±0.200	LEAD TIP TO TIP
4	D1	10.000±0.100	PKG LENGTH
5	E	12.000±0.200	LEAD TIP TO TIP
6	E1	10.000±0.100	PKG WDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H（REF）	(7.500)	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

Note: Dimensions are marked in millimeters.

Figure 17 LQFP64 - 64 Pins, 10 x 10mm Welding Layout Recommendations

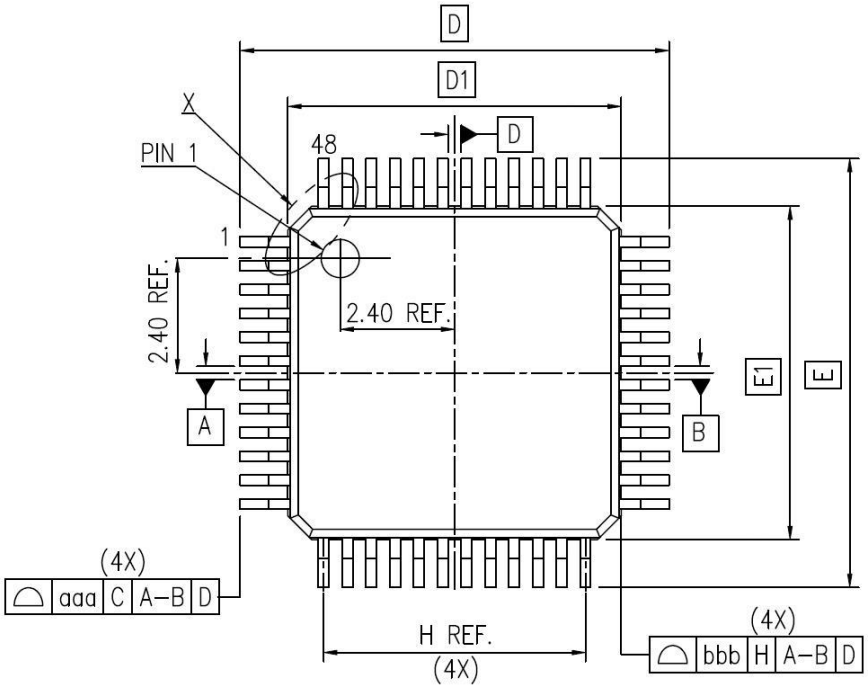


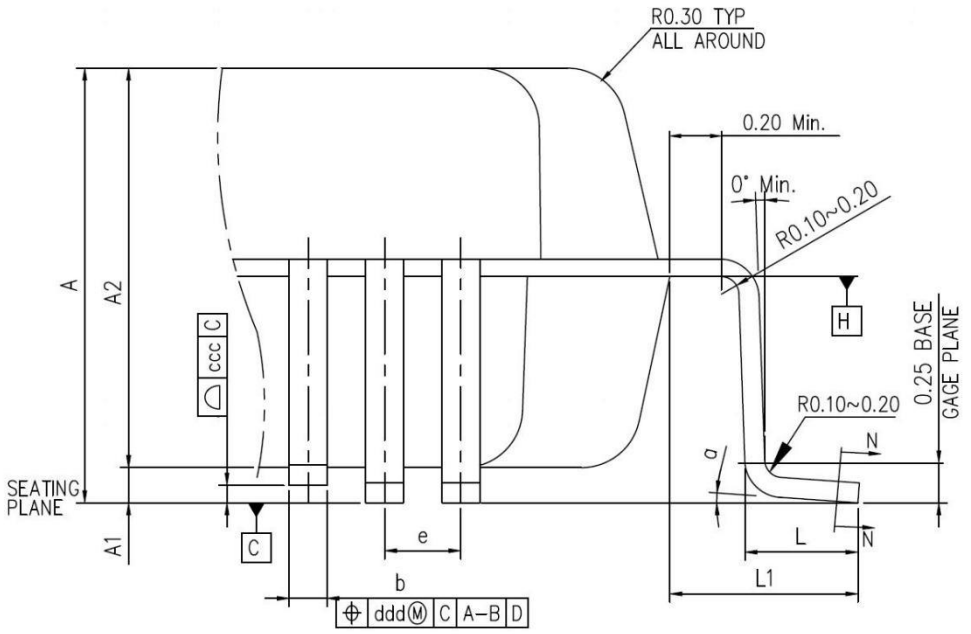
Note: Dimensions are marked in millimeters.

Figure 18 LQFP64 - 64 Pins, 10 x 10mm Package Identification

6.2 LQFP48 Package Diagram

Figure 19 LQFP48 Package Diagram





Note:

(1) The figure is not drawn to scale.

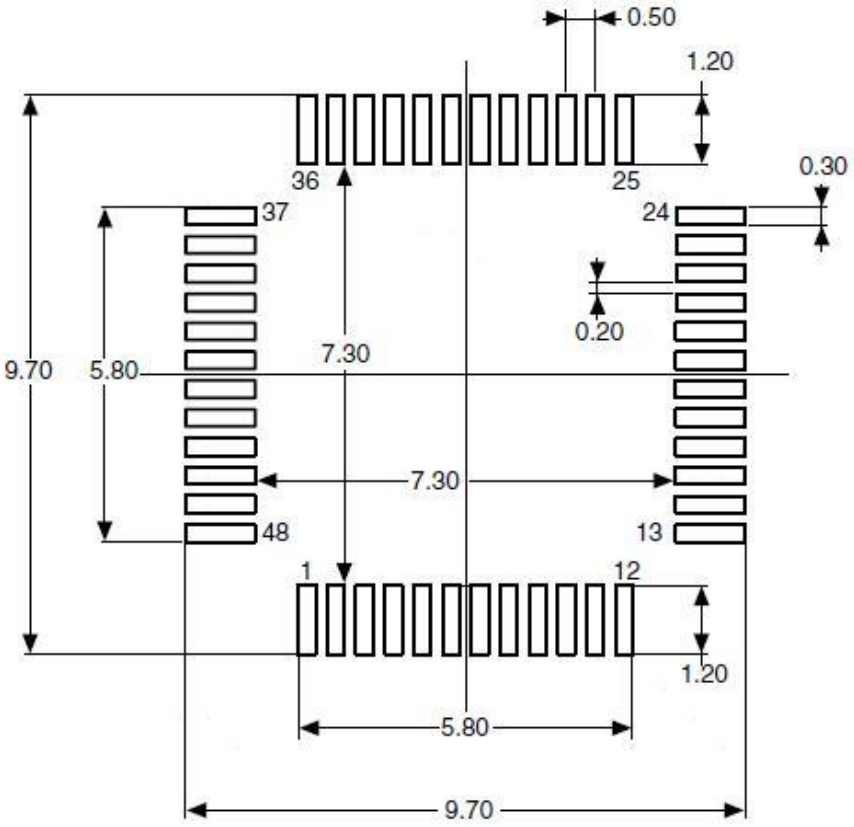
(2) All pins should be soldered to the PCB.

Table 50 LQFP48 Package Data

DIMENSION LIST(FOOTPRINT: 2.00)			
S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.60	OVERALL HEIGHT
2	A1	0.1±0.05	STANDOFF
3	A2	1.40±0.05	PKG THICKNESS
4	D	9.00±0.20	LEAD TIP TO TIP
5	D1	7.00±0.10	PKG LENGTH
6	E	9.00±0.20	LEAD TIP TO TIP
7	E1	7.00±0.10	PKG WDTH
8	L	0.60±0.15	FOOT LENGTH
9	L1	1.00 REF	LEAD LENGTH
10	T	0.15	LEAD THICKNESS
11	T1	0.127±0.03	LEAD BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.22±0.02	LEAD WIDTH
14	b1	0.20±0.03	LEAD BASE METAL WIDTH
15	e	0.50 BASE	LEAD PITCH
16	H(REF.)	(5.50)	CUM. LEAD PITCH
17	aaa	0.2	PROFILE OF LEAD TIPS
18	bbb	0.2	PROFILE OF MOLD SURFACE
19	ccc	0.08	FOOT COPLANARITY
20	ddd	0.08	FOOT POSITION

Note: Dimensions are marked in millimeters.

Figure 20 LQFP48, 7x7mm Welding Layout Recommendations

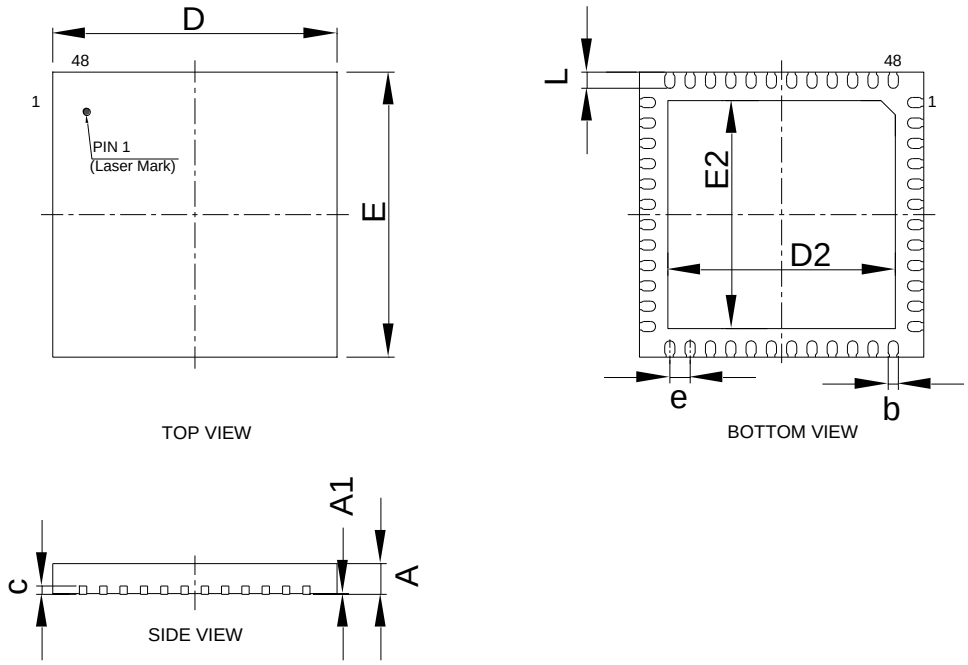


Note: Dimensions are marked in millimeters.

Figure 21 LQFP48 -48 Pins, 7x7mm Identification

6.3 QFN48 Package Diagram

Figure 22 QFN48 Package Diagram



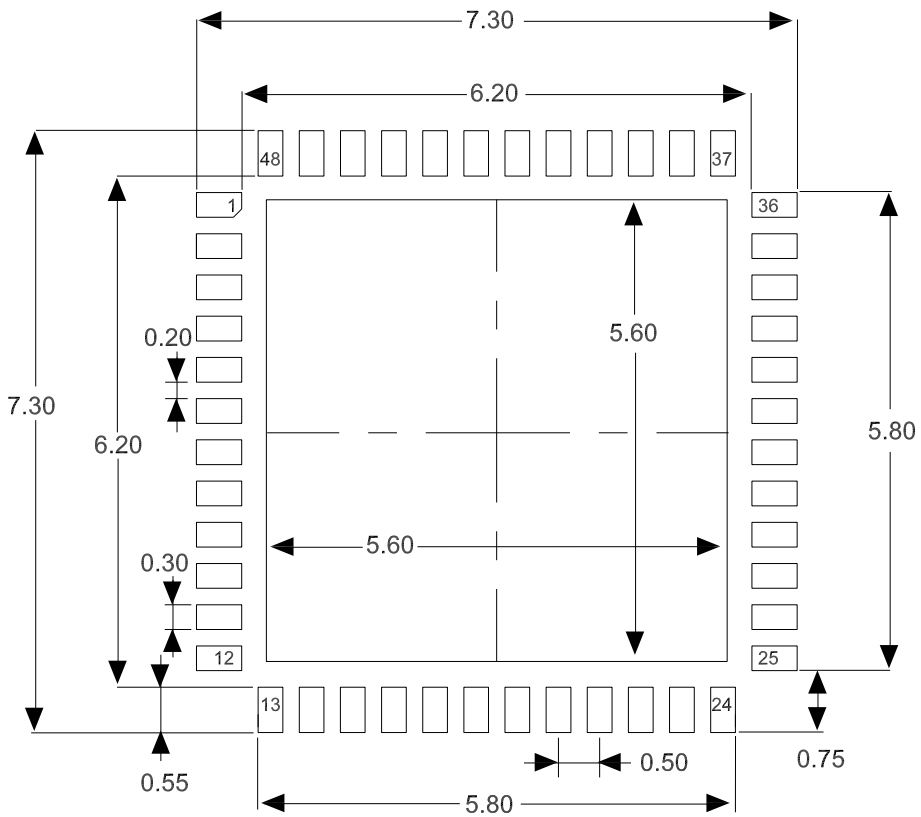
Note: The figure is not drawn to scale.

Table 51 QFN48 Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
c	0.203REF		
e	0.50BSC		
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
E	6.90	7.00	7.10
E2	5.50	5.60	5.70
L	0.35	0.40	0.45

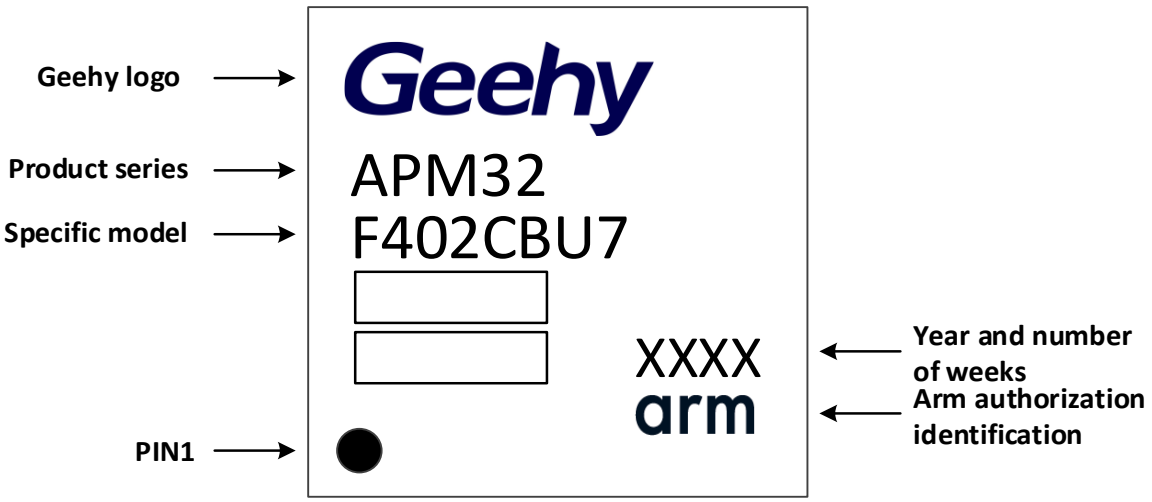
Note: Dimensions are marked in millimeters.

Figure 23 QFN48 Welding Layout Recommendations



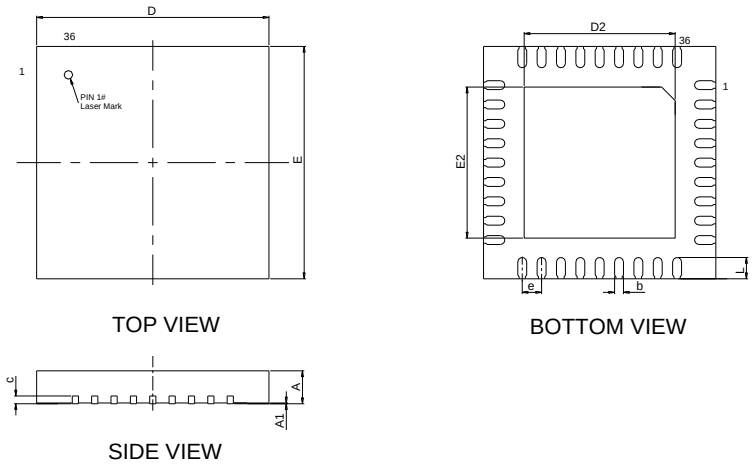
Note: Dimensions are marked in millimeters.

Figure 24 LQFP48-48 Pin 7x7mm Identification



6.4 QFN36 Package Diagram

Figure 25 QFN36 Package Diagram



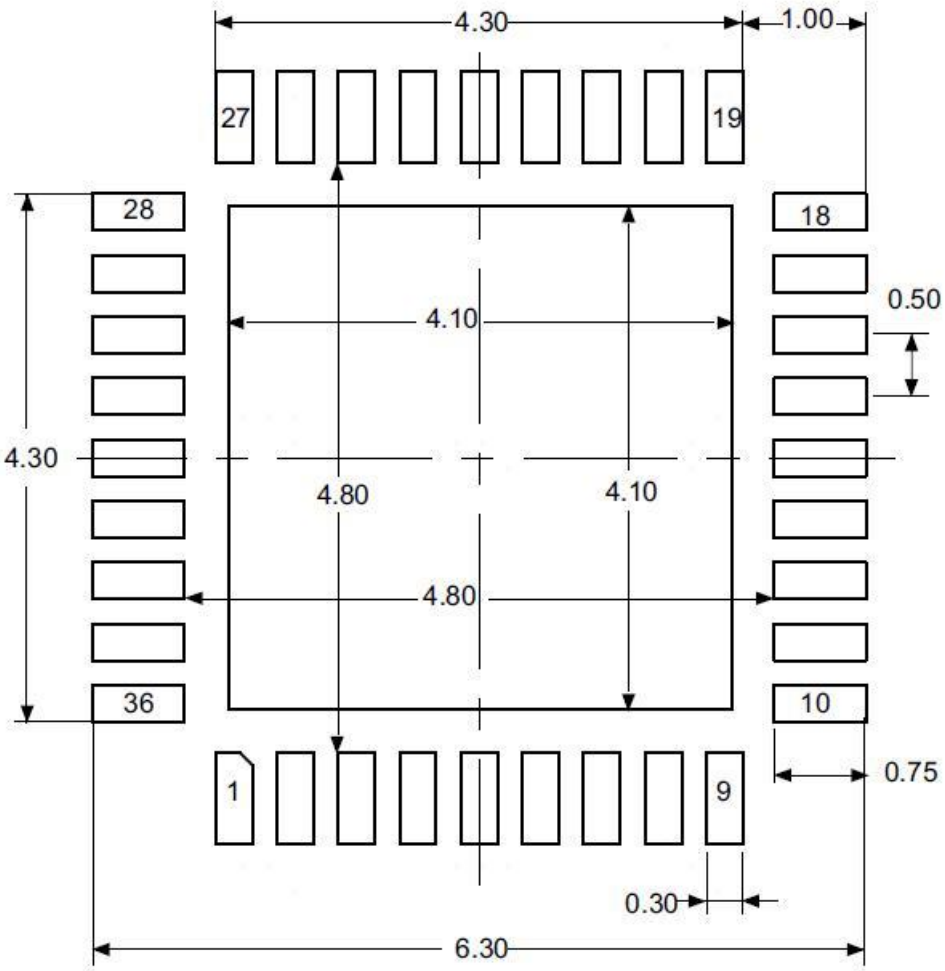
Note: The figure is not drawn to scale.

Table 52 QFN36 Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	3.80	3.90	4.00
E	5.90	6.00	6.10
E2	3.80	3.90	4.00
L	0.35	0.40	0.45
b	0.18	0.23	0.30
e	0.50		

Note: Dimensions are marked in millimeters.

Figure 26 QFN36 Welding Layout Recommendations



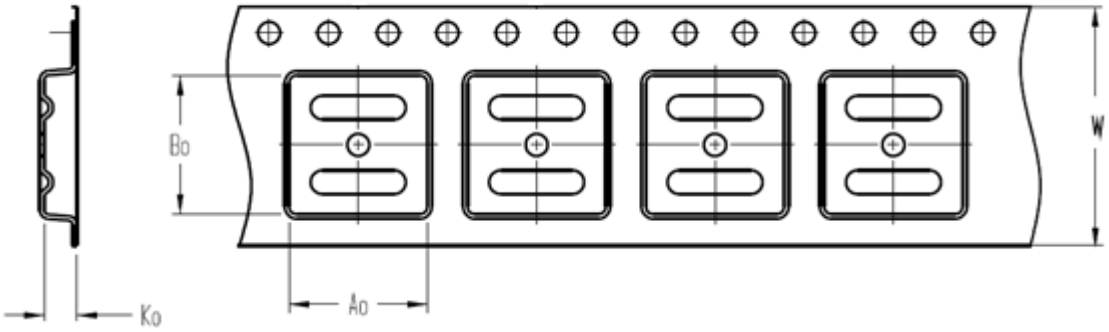
Note: Dimensions are marked in millimeters.

Figure 27 LQFN36-36 Pin 6x6mm Identification

7 Packaging Information

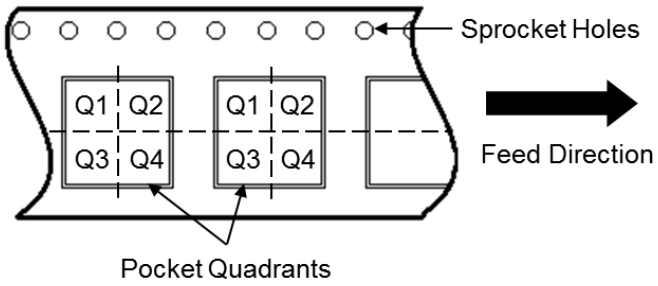
7.1 Reel packaging

Figure28Reel Packaging Specification Drawing

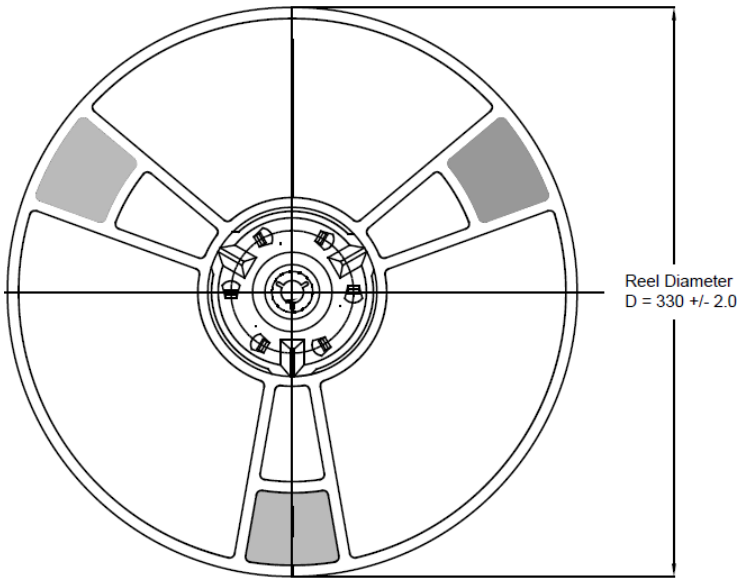


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions



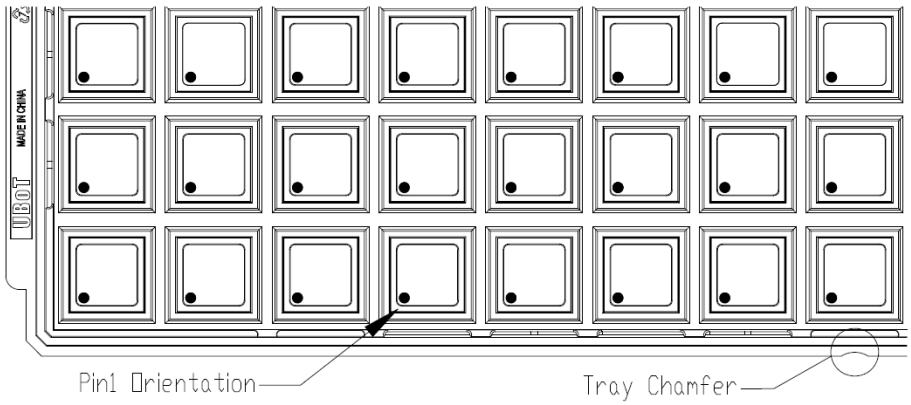
All photos are for reference only, and the appearance is subject to the product.

Table 53 Parameter Specification Table of Reel Packaging

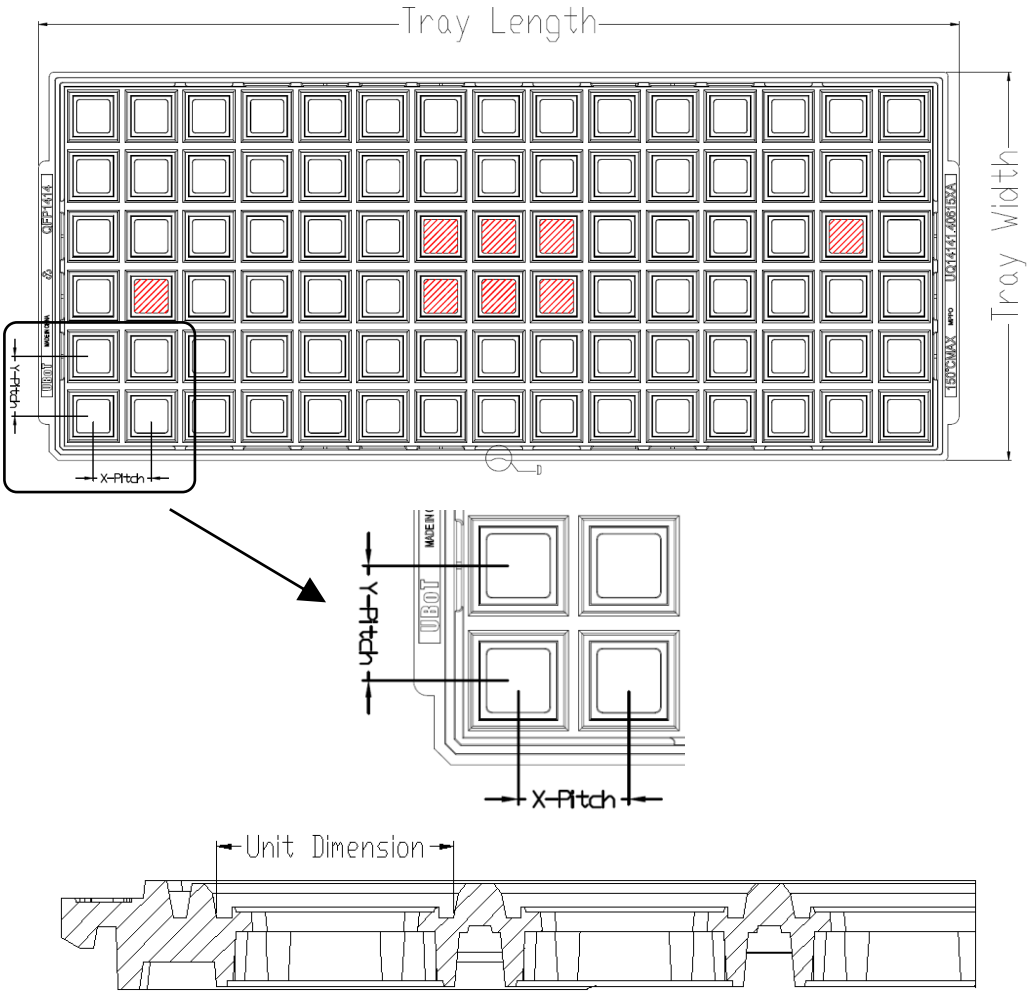
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
APM32F402RBT6	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
APM32F402CBT6	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1
APM32F402RBT7	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
APM32F402CBT7	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1

7.2 Pallet packaging

Figure 29 Pallet Packaging Diagram



Tray Dimensions



All photos are for reference only, and the appearance is subject to the product

Table 54 Parameter Specification Table of Pallet Packaging

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
APM32F402RBT6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F402CBT6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F402CBU6	QFN	48	2600	7.25	7.25	11.8	12.8	322.6	135.9
APM32F402TBU6	QFN	36	4900	6.2	6.2	8.8	9.2	322.6	135.9
APM32F402RBT7	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F402CBT7	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F402CBU7	QFN	48	2600	7.25	7.25	11.8	12.8	322.6	135.9
APM32F402TBU7	QFN	36	4900	6.2	6.2	8.8	9.2	322.6	135.9

8 Ordering Information

Figure 30 Product Naming Rules

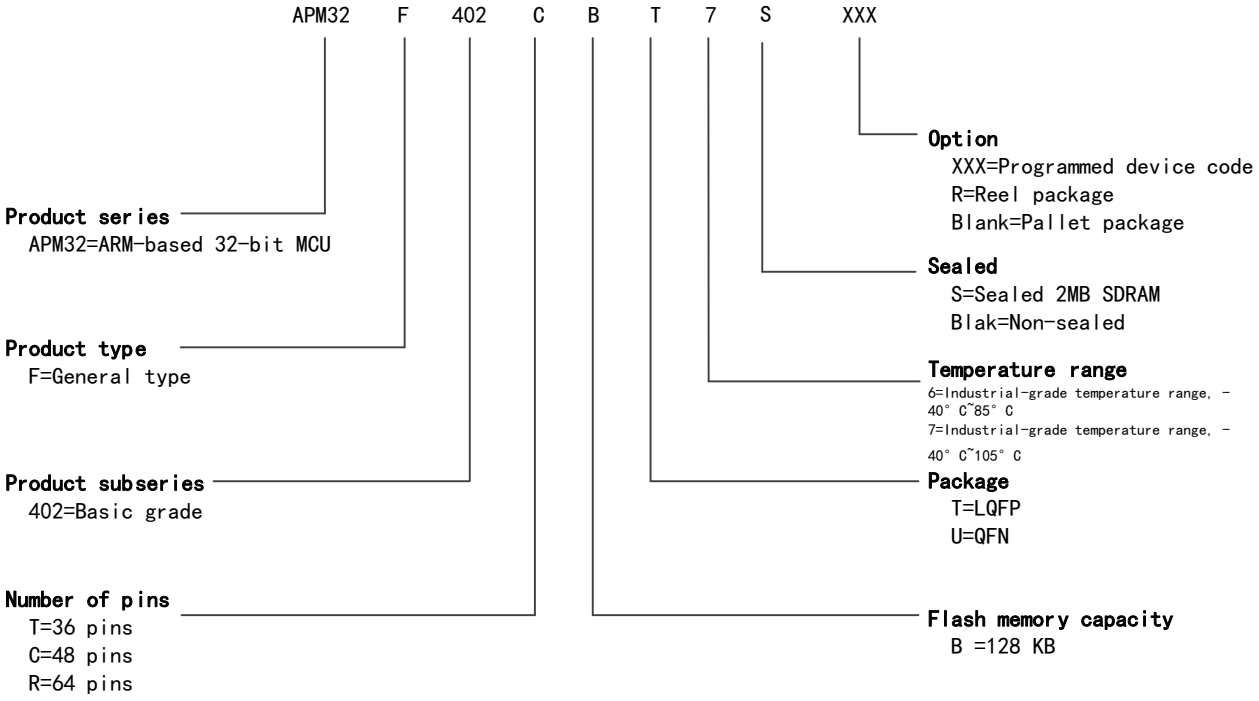


Table 55Ordering Information List

Order Code	FLASH（KB）	SRAM（KB）	Package	SPQ	Temperature range
APM32F402TBU6	128	32	QFN36	4900	Industrial grade -40℃~85℃
APM32F402CBU6	128	32	QFN48	2600	Industrial grade -40℃~85℃
APM32F402CBT6	128	32	LQFP48	2500	Industrial grade -40℃~85℃
APM32F402RBT6	128	32	LQFP64	1600	Industrial grade -40℃~85℃
APM32F402TBU7	128	32	QFN36	4900	Industrial grade -40℃~105℃
APM32F402CBU7	128	32	QFN48	2600	Industrial grade -40℃~105℃
APM32F402CBT7	128	32	LQFP48	2500	Industrial grade -40℃~105℃
APM32F402RBT7	128	32	LQFP64	1600	Industrial grade -40℃~105℃

9 Commonly Used Function Module Denomination

Table 56 Commonly Used Function Module Denomination

Chinese description	Abbreviation
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCM
External Interrupt	EINT
General-purpose IO	GPIO
Multiplexing IO	AFIO
Wake-up controller	WUPT
Buzzer	BUZZER
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC Controller	CRC
Power management unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Real-time Clock	RTC
External memory controller	EMMC
Controller Area Network	CAN
I2C Interface	I2C
Serial Peripheral Interface	SPI
Universal asynchronous receiver transmitter	UART
Universal synchronous and asynchronous receiver transmitter	USART
Flash interface control unit	FMC

10 Revision history

Table 57 Document Revision History

Date	Version	Revision History
February, 2025	1.0	New
June, 2025	1.1	（1） Add attention points under general operating conditions （2） Add power-on/power-off characteristics

Statement

This document is formulated and published by Geehy Semiconductor Co., Ltd. (hereinafter referred to as “Geehy”). The contents in this document are protected by laws and regulations of trademark, copyright and software copyright. Geehy reserves the right to make corrections and modifications to this document at any time. Read this document carefully before using Geehy products. Once you use the Geehy product, it means that you (hereinafter referred to as the “users”) have known and accepted all the contents of this document. Users shall use the Geehy product in accordance with relevant laws and regulations and the requirements of this document.

1. Ownership

This document can only be used in connection with the corresponding chip products or software products provided by Geehy. Without the prior permission of Geehy, no unit or individual may copy, transcribe, modify, edit or disseminate all or part of the contents of this document for any reason or in any form.

The “极海” or “Geehy” words or graphics with “®” or “™” in this document are trademarks of Geehy. Other product or service names displayed on Geehy products are the property of their respective owners.

2. No Intellectual Property License

Geehy owns all rights, ownership and intellectual property rights involved in this document.

Geehy shall not be deemed to grant the license or right of any intellectual property to users explicitly or implicitly due to the sale or distribution of Geehy products or this document.

If any third party’s products, services or intellectual property are involved in this document, it shall not be deemed that Geehy authorizes users to use the aforesaid third party’s products, services or intellectual property. Any information regarding the application of the product, Geehy hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party, unless otherwise agreed in sales order or sales contract.

3. Version Update

Users can obtain the latest document of the corresponding models when ordering Geehy products.

If the contents in this document are inconsistent with Geehy products, the agreement in the sales order or the sales contract shall prevail.

4. Information Reliability

The relevant data in this document are obtained from batch test by Geehy Laboratory or cooperative third-party testing organization. However, clerical errors in correction or errors caused by differences in testing environment may occur inevitably. Therefore, users should understand that Geehy does not bear any responsibility for such errors that may occur in this document. The relevant data in this document are only used to guide users as performance parameter reference and do not constitute Geehy's guarantee for any product performance.

Users shall select appropriate Geehy products according to their own needs, and effectively verify and test the applicability of Geehy products to confirm that Geehy products meet their own needs, corresponding standards, safety or other reliability requirements. If losses are caused to users due to user's failure to fully verify and test Geehy products, Geehy will not bear any responsibility.

5. Legality

USERS SHALL ABIDE BY ALL APPLICABLE LOCAL LAWS AND REGULATIONS WHEN USING THIS DOCUMENT AND THE MATCHING GEEHY PRODUCTS. USERS SHALL UNDERSTAND THAT THE PRODUCTS MAY BE RESTRICTED BY THE EXPORT, RE-EXPORT OR OTHER LAWS OF THE COUNTRIES OF THE PRODUCTS SUPPLIERS, GEEHY, GEEHY DISTRIBUTORS AND USERS. USERS (ON BEHALF OR ITSELF, SUBSIDIARIES AND AFFILIATED ENTERPRISES) SHALL AGREE AND PROMISE TO ABIDE BY ALL APPLICABLE LAWS AND REGULATIONS ON THE EXPORT AND RE-EXPORT OF GEEHY PRODUCTS AND/OR TECHNOLOGIES AND DIRECT PRODUCTS.

6. Disclaimer of Warranty

THIS DOCUMENT IS PROVIDED BY GEEHY "AS IS" AND THERE IS NO WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, TO THE EXTENT PERMITTED BY APPLICABLE LAW.

GEEHY'S PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED FOR USE AS CRITICAL COMPONENTS IN MILITARY, LIFE-SUPPORT, POLLUTION CONTROL, OR HAZARDOUS SUBSTANCES MANAGEMENT SYSTEMS, NOR WHERE FAILURE COULD RESULT IN INJURY, DEATH, PROPERTY OR ENVIRONMENTAL DAMAGE.

IF THE PRODUCT IS NOT LABELED AS "AUTOMOTIVE GRADE," IT SHOULD NOT BE CONSIDERED SUITABLE FOR AUTOMOTIVE APPLICATIONS. GEEHY ASSUMES NO LIABILITY FOR THE USE BEYOND ITS SPECIFICATIONS OR GUIDELINES.

THE USER SHOULD ENSURE THAT THE APPLICATION OF THE PRODUCTS COMPLIES WITH ALL RELEVANT STANDARDS, INCLUDING BUT NOT LIMITED TO SAFETY, INFORMATION SECURITY,

AND ENVIRONMENTAL REQUIREMENTS. THE USER ASSUMES FULL RESPONSIBILITY FOR THE SELECTION AND USE OF GEEHY PRODUCTS. GEEHY WILL BEAR NO RESPONSIBILITY FOR ANY DISPUTES ARISING FROM THE SUBSEQUENT DESIGN OR USE BY USERS.

7. Limitation of Liability

IN NO EVENT, UNLESS REQUIRED BY APPLICABLE LAW OR AGREED TO IN WRITING WILL GEEHY OR ANY OTHER PARTY WHO PROVIDES THE DOCUMENT AND PRODUCTS "AS IS", BE LIABLE FOR DAMAGES, INCLUDING ANY GENERAL, SPECIAL, DIRECT, INCIDENTAL OR CONSEQUENTIAL DAMAGES ARISING OUT OF THE USE OR INABILITY TO USE THE DOCUMENT AND PRODUCTS (INCLUDING BUT NOT LIMITED TO LOSSES OF DATA OR DATA BEING RENDERED INACCURATE OR LOSSES SUSTAINED BY USERS OR THIRD PARTIES). THIS COVERS POTENTIAL DAMAGES TO PERSONAL SAFETY, PROPERTY, OR THE ENVIRONMENT, FOR WHICH GEEHY WILL NOT BE RESPONSIBLE.

8. Scope of Application

The information in this document replaces the information provided in all previous versions of the document.